Code No: **R42046** **R10** **Set No. 1**

IV B.Tech II Semester Regular Examinations, April/May - 2014

STRUCTURED DIGITAL DESIGN

(Common to Electronics & Communication Engineering and Electronics & Computer Engineering)

Time : 3 hours **Max. Marks: 75**

Answer any Five Questions
All Questions carry equal marks
*****

1 a) Explain top-down design methodology with example. [8]
b) Define the term "Verilog as HDL". [7]

2 a) Explain the following with declaration format and an example each:
i) Variable ii) Signal iii) Constant [8]
b) Explain structural and behavioral description with examples. [7]

3 a) Write a VHDL code to implement a 2:4 decoder with an active low enable line? [8]
b) Write a VHDL code for 8:3 encoder operations? [7]

4 a) Draw the structure of a 8-bit counter. Write a VHDL description for an 8-bit counter. [8]
b) Write a behavioral description of JKFF with active low preset and clear inputs. [7]

5 Define the following terms relevant to Verilog HDL
a) Parameters b) Strings
c) Data types d) Concurrency [15]

6 a) Design verilog code of OR gate using **for** and **disable**. Write simulation results with explanation? [8]
b) Explain NAND gate primitive with verilog module? [7]

7 a) Perform the realization of state machine charts by considering a simple example. Give the fundamentals of state machine charts. [8]
b) Explain about synthesis process. [7]

8 a) Explain about the computer aided design tools. [8]
b) Classify the fault detection experiments for the sequential circuits. [7]

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1 a) Explain in brief the evolution of VHDL and mention the capabilities of the language. [8]

b) Discuss the design process of HDL? [7]

2 a) Give the classification of Data Types in VHDL. Explain Scalar type of data with an example. [8]

b) Explain assert statement and report statement. Give examples. [7]

3 a) Starting from a single bit full adder as a component, write down the structural VHDL description for a 4 bit adder? [8]

b) Write a VHDL program to model a 4-bit comparator. [7]

4 a) Write a VHDL code to implement a synchronous counter having the counting sequence as 2,0,3,1,2,0,3,1,…… using T-FF. [8]

b) Write a VHDL code for flip-flop with Rise/Fall time modeling using generic statement. [7]

5 Define the following terms relevant to Verilog HDL

a) Test bench

b) Simulation tools

c) Module

d) PLI [15]

6 a) Design a verilog module for a Multiplexer module at the data flow level. [7]

b) Explain net delay with assignment delay and effects of net delay with suitable examples. [8]

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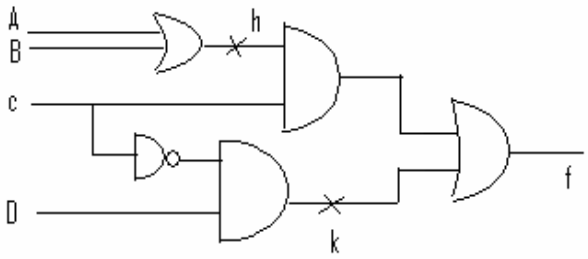
7 a) Write a VHDL code and synthesize the circuit for case statement. [8]
b) State the differences between synthesis of combinational logic and synthesis of sequential logic. [7]

8 a) Write a note on Built in self test? [8]
b) For the circuit shown below find tests to detect the faults h SAO and hSA1, K SAO and K SA1. Find tests to distinguish between the above faults.



[7]

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1 What is the need for CAD tools? With reference to CAD tools discuss,
a) Design entity b) Functional simulation c) Physical design [15]

2 a) Describe the following with a suitable example
i) Symbol Vs Entity ii) Configuration [8]
b) Explain the structure of process statement with a suitable example? [7]

3 a) Explain DATAFLOW style and BEHAVIORAL style of modeling in VHDL with an example of Z=A/B+AC. Develop suitable VHDL code. [8]
b) Differentiate between the conditional assignment statement and signal assignment statement with respect to 4:1 Mux. [7]

4 a) Discuss general model of mealy sequential machine. How do you realize mealy sequential network with a ROM? [7]
b) Write a VHDL description for a SR latch
i) Use a conditional assignment statement
ii) Use a characteristic equation
iii) Use two logic gates [8]

5 a) What is operator overloading? Give the different Operators available in Verilog. [8]
b) Write about different scalars and vectors in verilog module, with examples. [7]

6 a) Model the circuit of a Priority encoder using primitive gates. Output is 0 when all inputs are 0; otherwise it is a 1.Write a test bench and verify that the model behaves as a priority encoder. [8]
b) Explain Continuous assignment structures relevant to dataflow modeling with suitable examples. [7]

7 a) With suitable example explain the synthesis of sequential logic with latches. [7]
b) Give the differences between Explicit and Implicit state machines. [8]

8 a) What are the different faults found in combinational circuits? How can they be categorized? [7]
b) With an example, explain the principle of operation of path sensitizations method [8]

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*****

1 a) With the help of a block diagram, explain the stages of compilation, elaboration and simulation. [8]
b) Bring out differences between a VHDL and Verilog. [7]

2 a) Explain the terms entity, is, port, in, out and end pertaining to VHDL compiler. Write a VHDL program using all the above terms and explain the same. [8]
b) Write a note on packages. [7]

3 a) Write a VHDL code to implement a 3:8 decoder with an active low enable line using i) Conditional signal assignment
ii) Selected signal assignment statement [8]
b) Write a VHDL code for synthesis of a sequential IF statement. [7]

4 Design an 8-bit serial-in and serial-out shift register with flip-flops. Explain the operation with the help of timing waveforms. Write the dataflow style VHDL program for this shift register. [15]

5 a) Give the differences between Combinational logic design and Sequential logic design? [8]
b) What are inertial and transport delay models. Give their syntax and illustrate the difference between the two models. [7]

6 Realize each of the flip-flops below using NOR gates. Prepare a module and a test bench for flip-flops: RS flip flop; D-latch; clocked RS flip flop; Edge triggered D flip flop; Master –slave flip flop. [15]

7 a) Explain IEEE-1164 standard logic system for use with VHDL taking one VHDL code example. [8]
b) With suitable example explain the synthesis of sequential logic with flip-flop. [7]

8 a) Explain about the printed circuit boards? [7]
b) What are the different types of faults and give some examples for each type? [8]