Code No: R21054 **R10** SET - 1

II B. Tech I Semester Supplementary Examinations, Jan - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the given gray code number to equivalent binary 1001001011110010.
   b) Convert $(A0F9.0EB)_{16}$ to decimal, binary, octal.

2. a) What is meant by 'min-term' and 'max-term'? Write the procedure to obtain the canonical SOP form of a given logic functions.
   b) Express the following functions in sum of min-terms and product of max-terms.
   i) (xy+z) (y+xz) ii) B'D+A'D+BD

3. Obtain the minimal SOP expression for the switching function using k-map.
   $Y = \sum m(1,5,7,13,14,15,17,18,21,22,25,29) + \sum d(6,9,19,23,30)$
   Draw and explain the logic diagram

4. a) Draw the schematic diagram and truth table for half adder. Explain the design approach for half adder using universal gates. Draw the logic diagrams with relevant expressions.
   b) Design, draw and explain a 4-bit binary carry look ahead adder.

5. a) Describe the operations performed by the following logic circuits with an example
   i) Comparator ii) Decoder iii) Encoder
   b) Explain the operation of a 3-to-8 decoder 74LS138. Realize 4-to-16 decoder using two 3-to-8 decoders.

6. a) Using PLA logic, implement a BCD to excess-3 code converter. Draw and explain its truth table and logic diagram.
   b) Explain in brief, about logic construction of 32x4 ROM. Draw and explain the relevant logic diagram.

7. a) What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.
   b) Draw and explain the circuit diagram of positive edge triggered J-K flip-flop using NOR gates with its truth table. How race around conditions are eliminated?

8. a) Discuss about synchronous and ripple counters. Compare their merits and demerits.
   b) What do you mean by universal shift register? Draw and explain its circuit diagram and operation.
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Code No: R21054 **R10** SET - 2

II B. Tech I Semester Supplementary Examinations, Jan - 2015
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Time: 3 hours Max. Marks: 75

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1. a) Solve for x
   i) $(367)_8=(x)_2$ ii) $(378.93)_{10}=(x)_8$ iii) $(B9F.AE)_{16}=(x)_8$ iv) $(16)_{10}=(100)_x$
   b) Convert $(163.875)_{10}$ to binary, octal, hexadecimal.

2. a) What are universal gates? Realize AND, OR, NOT, XOR gates using universal gates.
   b) Obtain the canonical SOP form of the following functions.
   i) Y(A,B) = A+B ii) Y(A,B,C,D) = AB+ACD

3. a) Simplify the expression $Y=\sum m(7,9,10,11,12,13,14,15)$ using the k-map method.
   b) Simplify the following Boolean function, $F(A,B,C,D)=\sum m(1,3,7,11,15)+\sum d(0,2,5)$

4. a) Draw the schematic diagram and truth table for full adder. Explain the design approach for full adder using universal gates. Draw the relevant logic diagrams with necessary expressions.
   b) Draw and explain the operation of 2's complement adder-subtractor

5. a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers.
   b) Realize the function $f(A,B,C,D)=\pi(1,4,6,10,14)+d(0,8,11,15)$ using
   i) 16:1 MUX ii) 8:1 MUX

6. a) Tabulate the PLA programming table for the following Boolean functions.
   $F_1(x,y,z)=\sum m(0,2,3,7)$
   $F_2(x,y,z)=\sum m(1,3,4,6)$
   $F_3(x,y,z)=\sum m(1,4)$
   Draw and explain the relevant logic diagram. (8M)
   b) Design, draw and explain 128 × 8 ROM using 32×8 ROM.

7. a) Realize D-FF and T-FF using JK-FF. Draw the logic diagrams with their truth tables.
   b) Deduce the design procedure for sequential logic circuits and give the classification of sequential logic circuits.

8. a) Design, draw and explain a synchronous MOD-12 down-counter using j-k flip-flop.
   b) Design, draw and explain a 4-bit ring counter using D- flip flops with relevant timing diagrams.
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Code No: R21054 **R10** SET - 3

II B. Tech I Semester Supplementary Examinations, Jan - 2015
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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
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1. a) Solve for x
   i) $(257)_8 = (x)_2$ ii) $(21.625)_{10} = (x)_8$ iii) $(BC.2)_{16} = (x)_8$ iv) $(33)_{10} = (201)_x$
   b) Express the Decimal Digits 0-9 in BCD, 2421, 8421 and Excess-3.

2. a) Prove the following Boolean theorems
   i) AB+A'C = (A+C)(A'+B) ii) AB+A'C+BC = AB+A'C
   b) Simplify the following Boolean expressions
   i) ABC+AB'+ABC' ii) ACD+A'BCD.

3. a) Simplify the expression Y= π (7, 9, 10, 11, 12, 13, 14, 15) using the k-map method.
   b) Simplify the expression Y= $m_1 + m_5 + m_{10} + m_{11} + m_{12} + m_{13} + m_{15}$ using the k-map method.

4. a) Draw the block schematic and truth table for full-subtractor. Explain the design approach for full-subtractor with two half-subtractors. Draw the relevant logic diagram with necessary expressions.
   b) Draw and explain the operation of carry look ahead adder.

5. a) Implement full adder with 4 to 1 multiplexer.
   b) Implement 64 x 1 multiplexer with four 16 x 1 and one 4 x 1 multiplexer.

6. a) Derive the PLA programming table for the combinational circuit that squares a 3-bit number. Draw the relevant logic diagram.
   b) A ROM chip of 4,096 × 8 bits has two chip select inputs and operates from a 5-volt power supply. How many pins are needed for the integrated circuit package? Draw and explain the relevant block diagram.

7. a) Explain the sequential logic circuits and clocked sequential logic circuits with relevant examples.
   b) Design SR latch with universal logic gates. Draw and explain the logic diagrams.

8. a) Design, draw and explain the 4-bit universal shift register.
   b) Describe the parallel-in serial-out shift register with logic diagram. Give the design considerations.
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Code No: R21054 **R10** SET - 4

II B. Tech I Semester Supplementary Examinations, Jan - 2015
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Time: 3 hours Max. Marks: 75

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1. a) Covert (105.15_{10}) to binary, octal, hexadecimal.
   b) What is hamming code? How is the hamming code word tested and corrected.

2. a) Simplify the following Boolean expressions using the Boolean theorems.
   i) (A+B+C) (B'+C) + (A+D) (A'+C) ii) (A+B) (A+B') (A'+B)
   b) Why NAND and NOR gates are known as universal gates? Simulate all the gates.

3. a) Simplify Y = ∑ m(3,6,7,8,10,12,14,17,19,20,21,24,25,27,28) using K-map method.
   b) Obtain i) minimal SOP and ii) minimal POS expressions for the following function.
   F(A,B,C,D)= ∑ m(0,1,5,8,9,10)

4. a) Present the steps involved in the design procedure of a combinational circuit. Consider a suitable example.
   b) Design, draw and explain the operation of ripple adder.

5. a) Explain the differences between a MUX and a DEMUX. Realize 16-input multiplexer by cascading of two 8-input multiplexers 74151.
   b) Realize the function f(A,B,C,D) = ∑m(1,2,5,8,10,14) + d(6,7,15) using
   i) 16:1 MUX ii) 8:1 MUX.

6. a) Give the logic implementation of a 32×4 bit ROM using decoder of suitable size.
   b) Implement the following Boolean function with PLA F(A,B,C) = ∑ m(1,5,6,7)

7. a) Explain the operation R-S master slave flip flop. Explain its truth table
   b) Explain about the realization of SR flip-flop, JK flip-flop using D flip-flop.

8. a) Design, draw and explain a modulo -12 up synchronous counter using T- flip flops.
   b) Draw and explain the logic diagram for a 4-bit binary ripple down counter using positive edge triggered flip-flops.
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