Code No: R21054 **R10** SET - 1

II B. Tech I Semester Supplementary Examinations, June - 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks

1 a) Convert the number $(17.125)_{16}$ to base 10, base 4 , base 5 and base 2.
b) Show that gray code is both reflective and unit distance code .

2 a) Explain any four basic theorems of algebra with necessary proofs.
b) Find the dual complement of $ABC + \bar{D}.E + B\bar{C}E$.

3 a) Draw 3-variable and 4-variable k-map and define pair , quad and octet.
b) Simplify the following function using k map
F(w,x,y,z) = $\sum$ (0,1,2,5,6,8,9) + $\sum_d$(3,10,11,15)

4 Design a combinational circuit to convert BCD to gray code.

5 a) What is an encoder? Design octal to binary encoder.
b) Realize F(w,x,y,z)= Σ (1,4,6,7,8,9,10,11,15) using 4 to 1 MUX.

6 a) Using PROM realize the following expression .
F_1(a,b,c)=Σ (0,1,3,5,7)
F_2(a,b,c)= Σ(1,2,5,6)
b) Derive the PLA programming table for the combinational circuit that squares a 3-bit number

7 a) Convert D flip-flop into T, JK and SR flip-flop.
b) Explain the operation of JK flip flop with the help of input output waveforms.

8 a) Show that a BCD ripple counter can be constructed using a 4-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.
b) Explain with the help of neat diagram, the operation of 3-bit bidirectional shift register.

Code No: R21054 **R10** SET - 2

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Answer any **FIVE** Questions
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1 a) Convert the following to decimal and then to binary
i)$(2311)_{16}$ ii)$(A44D)_{16}$ iii)$(7444)_8$ iv) $(7667)_8$ v) $(158)_{10}$
b) Explain about weighted and non-weighted codes with example

2 a) Find the dual of the following expressions
i) $x + (\overline{\bar{x}\bar{y} + \bar{x}z})$ ii) vwx+vwyz+wxy+vxyz
b) Explain the truth tables of X-OR , NAND,NOR gates.

3 a) Express the following equation in its minimal SOP from and realize it using 2 input NAND gate only $f = A + (\overline{\overline{A \oplus B} \oplus C})$
b) Find the minimal POS from using K-map for the following expression
F(w,x,y,z) =π (0,1,2,6,7,9) +π_d(3,4,8,9)

4 Design a combinational logic circuit that has 3 inputs. The output is required to go HIGH whenever the number of inputs have even number of 1's. Draw the truth table. Minimize the Boolean function using K-map. Draw the circuit diagram.

5 a) Explain the implementation of 4-input priority encoder with truth table, k-maps, Boolean function and schemantic diagrams.
b) Design a 4 to 1 MUX using a 2 to 4 decoder and basic gates.

6 a) Implement binary to excess 3 code converter using ROM
b) What is PLA? Explain the programming table of PLA. How is the size of a PLA specified

7 a) Draw the circuit diagram of clocked D-flip flop with NAND gates and explain its operation using truth table. Give its timing diagram.
b) Construct a JK flip-flop using a D flip-flop, a 2 to 1-line multiplexer and an inverters.

8 a) Explain Ring counter operation and its applications using a diagram
b) Explain with the help of neat diagram the operation of 4-bit universal shift register.
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Code No: R21054 **R10** SET - 3

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Answer any **FIVE** Questions
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1 a) Convert the number$(127.75)_8$ to base 10,base 3 , base 16 and base 2.

b) Explain subtraction in the 2`s complement system with suitable example.

2 a) Prove the identity of the following equations
i) $\bar{x}\bar{y} + \bar{x}y + xy = \bar{x} + y$ *ii)* $\bar{a}b + \overline{bc} + ab + \bar{b}c = 1$

b) Implement the INVERTER gate, OR gate and AND gate using NAND gate ,NOR gate.

3 a) Simplify the following function using K-map.
$F(A, B, C, D) = \Sigma(1,3,4,5,6,11,13,14,15)$

b) Find the prime implicants for the following and determine which are essential. F(w,x,y,z)=Σ(0,2,4,5,6,7,8,10,13,15) using K-map

4 a) What is half subtractor? Write its logic diagram and truth table

b) Explain carry propagation in parallel adder with a neat diagram.

5 a) Draw the circuit for 3 to 8 decoder and explain.

b) Implement the given function using multiplexer F(x,y,z) = Σ (0,2,6,7).

6 a) Given a 32x8 ROM chip with an enable input, show the external connection necessary to construct a 128x8 ROM with four chips and a decoder

b) How programmable logic array is advantageous over ROMs ? What is meant by an LSI device.

7 a) What do you mean by triggering? Explain the various triggering modes with examples.

b) Draw the logic diagram and write functional table of an SR latch using NAND gates. Explain the operation

8 a) Draw and explain the 4-bit shift register with necessary example.

b) Design a serial adder using JK flip-flop , shift register and logic gates.

Code No: R21054 **R10** SET - 4

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Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
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1 a) Determine the value of b for the following :
i)$(292)_{10}$ =$(1204)_b$ ii) $(16)_{10}$ = $(100)_b$
b) Explain the binary to Gray conversion with the help of examples.

2 a) Simplify the following Boolean functions to minimum number of literals,
$i) F = X'Y' + XYZ + X'Y$ $ii)\ F = X + Y[Z + (X + Z)']$
b) Implement $Y = AB' + CD + (A'B + C'D')$ using NAND gates.

3 a) Simplify the following function using map method.
$F = A'BC'D' + A'BC'D + AB'CD + AB'CD' + ABCD + A'B'C'D'$
b) For the given function $T(w, x, y, z) = \Sigma(0,1,5,7,8,10,14,15)$
i) Find all prime implicates and indicate which are essential.
ii) Find a minimal expression using k map and realize using basic gates.

4 Design an 8-bit BCD adder using 4-bit binary adder.

5 a) Explain how decoder can be converted into a demultiplexer with a neat block diagram.
b) Implement a full adder with two multiplexer.

6 a) Draw the block diagram of a ROM. Define address and word. Relate the number of output lines with number of bits in a word. How an output word can be selected
b) Give the block diagram of PLA. Which are the terms programmable? How inverter is useful in the PLA construction at the output.

7 a) Draw the logic diagram of an SR latch with control input using NAND gates
b) What is race around condition? How is it rectified in master-slave JK flip-flop?

8 a) What is a shift register classified? Explain about the following mode of operation i) shift right ii) shift left iii) bidirectional in a four bit shift register.
b) Draw the logic diagram of a 4-bit binary ripple counter using positive edge triggering.
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