Code No: R21054   **R10**   SET - 1

II B. Tech I Semester Supplementary Examinations, Dec- 2015
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours   Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following numbers with the indicated bases into decimal numbers: (8M)
   i)$(12121.12)_3$ ii)$(4310)_5$ iii)$(5AB.126)_{16}$
   b) What is 'r' s complement method and (r-1)'s complement method. Explain? (7M)

2. a) Realize EX-NOR gate using universal gates separately? (7M)

   b) Find the complement of the following Boolean expressions: (8M)
   i) $(A\bar{B} + C)D + E$ ii) $AB(\bar{C}D + C\bar{D}) + \bar{A}\bar{B}(\bar{C} + D)(C + \bar{D})$

3. a) Simplify the following Boolean function '*F*' together with the don't care condition d; (8M)
   Then express the simplified function in sum of minterms :
   i) $F(W,X,Y,Z) = \sum (0,1,2,4,5,11,12)$ given $d(X,Y,Z) = \sum (3,6,7,9)$
   b) Draw the logic diagram for the simplified above function? (7M)

4. a) Design a combinational logic circuit with three inputs and one output. Given that the output is equals to logic-1 when binary value of the input is less than 3. The output is logic-0 otherwise? (9M)
   b) Draw the block diagram and truth table for Half Adder? Explain it with a k-map? (6M)

5. a) Construct a 16 X 1 MUX with the help of two 8 X 1 MUX and one 2 X 1 MUX, use block diagram for multiplexer ? (8M)
   b) Explain clearly about Priority Encoder? (7M)

6. a) Explain the architecture of a PAL with the help of neat diagram ? (8M)
   b) How can a PLD be programmed by using a computer? Explain? (7M)

7. a) Realize the master slave D - flip flop using only NAND gates? (8M)
   b) Discuss clearly the SR to D flip flop conversion? (7M)

8. Write short notes on the following: i) Binary Ripple Counter ii) Ring Counter (15M)