Code No: **R31041** **R10** **Set No. 1**

III B.Tech I Semester Supplementary Examinations, June/July - 2015
COMPUTER ARCHITECTURE & ORGANIZATION
(Comm to ECE and EIE)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1	a)	Design a 4-bit adder/ subtracter circuit using full adders.	[8]
	b)	What are the special registers in a typical computer? Explain their purpose in detail.	[7]
2		What is an addressing mode? Describe various addressing modes that exit in a modern processor.	[15]
3	a)	Explain the execution of micro instructions with a neat diagram.	[5]
	b)	Briefly describe the design of a hardwired control unit.	[10]
4	a)	Explain the rules for basic arithmetic operations of floating point numbers. 8m	[8]
	b)	Describe with an example, how to multiply two unsigned binary numbers.	[7]
5	a)	What is cache memory? How its performance can be increased? Discuss.	[10]
	b)	Explain the method of translating virtual address to physical address.	[5]
6		What are the needs for input-output interface? Explain the functions of a typical 8-bit parallel interface in detail.	[15]
7		Explain Flynn's classification in detail.	[15]
8	a)	Give the system tree structure for multiprocessors.	[7]
	b)	Explain the inter processor communication mechanism in CM-5.	[8]

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Code No: **R31041** **R10** **Set No. 2**

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Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1	a)	Briefly explain about the integer arithmetic with suitable examples.	[8]
	b)	Draw and explain the block diagram of a complete processor.	[7]
2	a)	Explain the relation between pipelined execution and instruction execution.	[7]
	b)	Discuss the control sequence for conditional and unconditional branch Instructions.	[8]
3		Explain the design of micro-programmed control unit in detail.	[15]
4	a)	Discuss about Booth's multiplication algorithm.	[7]
	b)	Explain an algorithm for adding and subtracting two floating point binary numbers.	[8]
5	a)	What is a DRAM? Explain the types of DRAMs with suitable diagrams.	[10]
	b)	What is virtual memory? Give its merits and demerits.	[5]
6	a)	Describe the hardware mechanism for handling multiple interrupt requests.	[7]
	b)	How data transfer can be controlled using handshaking technique?	[8]
7	a)	What is meant by parallel processing? What is the basic objective of parallel processing?	[7]
	b)	Explain different types of vector instructions with neat diagram	[8]
8	a)	What are multiprocessors? Give their characteristics.	[7]
	b)	Briefly explain about Daisy- chain arbitration.	[8]

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Code No: **R31041** **R10** **Set No. 3**

III B.Tech I Semester Supplementary Examinations, June/July - 2015
COMPUTER ARCHITECTURE & ORGANIZATION
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Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1	a)	Draw the diagram of the single Bus Organization of the data path inside a processor	[7]
	b)	Describe the connections between the processor and memory with a Neat structure diagram	[8]
2	a)	How can memory access be made faster in a pipelined operation? Which hazards can be reduced by faster memory access?	[10]
	b)	Give the control sequence for the instruction ADD R4,R5,R6	[5]
3	a)	Explain the Organization of the control unit to allow conditional branching in the microprogram.	[8]
	b)	What is hard wired control? How is it different from micro programmed control?	[7]
4		Draw and explain the flowchart for division of two binary numbers using non-Restoring algorithm. Take the case of 8 divided by 5.	15]
5	a)	Explain various mapping techniques associated with cache memories.	[10]
	b)	What are the different secondary storage devices? Elaborate on any one of the devices.	[5]
6		Explain the working of PCI interface.	[15]
7		What is cache coherence problem? Explain the approaches to maintain consistent multi cache copies.	[15]
8	a)	With a neat diagram explain the internal organization of a processor.	[8]
	b)	What is arbitration? Briefly explain about dynamic arbitration algorithms.	[7]

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Code No: **R31041** **R10** **Set No. 4**

III B.Tech I Semester Supplementary Examinations, June/July - 2015
COMPUTER ARCHITECTURE & ORGANIZATION
(Comm to ECE and EIE)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
*****

1		Explain the design of an Arithmetic and Logic Unit in detail.	[15]
2		Explain how the following expression will be executed in one address, two address and three address processors in an accumulator organization X=AXB + CXC.	[15]
3		Explain the basic organization of a micro programmed control unit and the generation of control signals using micro program.	[15]
4		Explain Booth's algorithm. Apply Booth's algorithm to multiply the two decimal numbers 14 and 12. Assume the multiplier and multiplicand to be of 5 bits each	[15]
5	a)	Explain how the virtual address is converted into real address in a paged virtual memory system.	[8]
	b)	Analyze the memory hierarchy in terms of speed, size and Cost.	[7]
6	a)	With a neat diagram explain the working principles of DMA.	[8]
	b)	What are handshaking signals? Explain the handshake control of data transfer during input and output operation.	[7]
7		Write short notes on following: a) Non- uniform memory access b) Symmetric multiprocessors.	[15]
8		Briefly explain about communication and synchronization in multi processors.	[15]

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