Code No: **R31026** **R10** **Set No. 1**

III B.Tech I Semester Supplementary Examinations, May/June - 2015

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1	a)	Sketch a current mirror circuit and explain its operation. Show how a current mirror can be used as a constant current circuit for a differential amplifier. Explain the circuit operation and discuss its effect.	[8]
	b)	Explain the importance of level translator in an op amp.	[7]
2	a)	Why is it necessary to use an external offset voltage compensating network with practical op - amp circuits?	[4]
	b)	Compare and contrast an ideal op - amp and practical op - amp.	[6]
	c)	Define slew rate and what causes it. How is the slew rate measured?	[5]
3	a)	With suitable circuit diagram explain the operation of a triangular wave generator using a comparator and a integrator.	[8]
	b)	Explain the principle of operation of a precision full wave rectifier with waveforms	[7]
4	a)	Draw and explain the operation of Mono stable multivibrator using 555 timer. Derive the expression for time delay.	[8]
	b)	Draw the dc voltage versus phase difference characteristic of balanced modulator phase detector of a PLL indicating all important regions.	[7]
5	a)	Design a first order wide band-reject filter with a higher cut-off frequency of 100 Hz and a lower cut-off frequency of 1 kHz. Calculate the Q of the filter.	[8]
	b)	Sketch the circuit of a R-2R DAC, explain its operation, and calculate the analog output for any given digital input. Explain the performance of R-2R DAC comparing with that of the weighted-resistor DAC.	[7]
6	a)	Write short notes on priority encoder.	[8]
	b)	Explain the logic diagram and functional table of 4 to 1 line multiplexer.	[7]
7	a)	Design and implement a MOD-10 synchronous counter using J-K flip-flops.	[8]
	b)	Draw logical diagram of a 4-bit shift register. Explain how shift-left and shift-right operations are performed.	[7]
8	a)	Give the comparison between PROM, PLA and PAL.	[6]
	b)	Explain the functional behavior of Static RAM cell? Show the internal structure of 8×4 static RAM.	[9]

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Code No: **R31026** **R10** **Set No. 2**

III B.Tech I Semester Supplementary Examinations, May/June - 2015

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1	a)	Explain the classification of ICs according to their method of fabrication.	[8]
	b)	Discuss about dc analysis of Dual input balanced output amplifier.	[7]
2	a)	Define the Op-Amp parameters: i) Input offset Voltage, $V_{io,;}$ ii) Input bias current, I_{io} With a practical setup explain how these parameters can be measured.	[8]
	b)	Explain frequency compensation techniques used in op-amps.	[7]
3	a)	Draw & discuss the operation of a log amplifier with a circuit diagram. Derive the expression for output voltage.	[8]
	b)	Design a current to voltage converter using Op-amp and explain how it can be used to measure the output of a photocell.	[7]
4	a)	Design an Astable multivibrator using 555 timer for a frequency of 1 kHz and a duty cycle of 70%.Assume C=0.1µf.	[8]
	b)	Give the block diagram of NE 565 PLL and explain the role of each block. Make circuit connections to track the incoming signal and explain its operation.	[7]
5	a)	Write the advantages of active filter. Explain different configurations of active filter and discuss their merits and demerits.	[8]
	b)	What are servo-tracking A/D converters? Why are they called so? How is it better than counter type A/D converter?	[7]
6	a)	Realize 16 input multiplexer using two 8 input multiplexers.	[7]
	b)	Implement a 4 bit ripple adder using half-adders/full-adders.	[8]
7	a)	Design a modulo-100 counter using two 74×163 binary counters?	[8]
	b)	Design a 4 bit bidirectional shift register using D flip-flops (Use relevant digital ICs).	[7]
8	a)	Describe the difference between PLA & PAL using logic diagrams.	[8]
	b)	With the help of a circuit diagram, explain the read and write operations of a dynamic RAM cell. Differentiate between static RAM and dynamic RAM.	[7]

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Code No: **R31026** **R10** **Set No. 3**

III B.Tech I Semester Supplementary Examinations, May/June - 2015

LINEAR & DIGITAL IC APPLICATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1	a)	What are the three differential amplifier configurations? Compare and contrast these configurations.	[8]
	b)	Explain ac analysis of differential amplifier.	[7]
2	a)	List out the AC characteristics of an op-amp and discuss about them.	[8]
	b)	b) Define the terms, CMRR and input bias current. Describe the techniques used for the measurement of these parameters.	[7]
3	a)	Draw the circuit diagram of an integrator circuit and explain its functioning with the Input-output wave forms. Derive the output voltage V_0 of an integrator circuit.	[8]
	b)	Design a monostable multivibrator with trigger pulse shaping which will drive a LED ON for 0.5 sec each time it is pulsed.	[7]
4	a)	Draw the internal circuit diagram of a 555 timer IC and explain how does it functions as astable multivibrator.	[8]
	b)	Define the terms 'Lock range' 'Capture range' and 'Pull in time' pertaining to PLL. Derive the relationship between lock range and capture range through a mathematical expression.	[7]
5	a)	Design a second order Butterworth low-pass filter having upper cut-off frequency 2.5KHz.	[8]
	b)	Draw the schematic block diagram of dual-slope A/D converter and explain its operation. Derive expression for its o/p voltage 'V_0'.	[7]
6	a)	Design a BCD-to-excess-3 code converter with a BCD-to-decimal decoder and OR gates.	[8]
	b)	Draw the logic diagram of a 4-bit ALU and explain.	[7]
7	a)	Design a modulo-16 synchronous binary counter using J-K flip-flops.	[8]
	b)	Design a 8-bit parallel-in and serial-out shift register? Explain the operation of the above shift register with the help of timing waveforms?	[7]
8	a)	Discuss in detail ROM access mechanism with the help of timing waveforms?	[8]
	b)	Explain the internal structure of 64K×1 DRAM. With the help of timing waveforms discuss DRAM access.	[7]

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Code No: **R31026** **R10** **Set No. 4**

III B.Tech I Semester Supplementary Examinations, May/June - 2015

LINEAR & DIGITAL IC APPLICATIONS

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1	a)	Draw and explain the internal block schematic of an operational amplifier.	[8]
	b)	Explain different methods to increase the input resistance of an op-amp.	[7]
2	a)	Describe non ideal dc characteristics which add error components to the dc output voltage of an op-amp.	[8]
	b)	Explain Pole-zero compensation technique for an op-amp and give its comparison with other compensation techniques.	[7]
3	a)	Explain the operation of an op-amp based monostable multivibrator.	[8]
	b)	Sketch& explain the circuit operation of log and antilog amplifiers. Calculate output voltages for a given input and show how temperature dependence is minimized.	[7]
4	a)	Explain the operation of Schmitt trigger using 555 timer with its circuit diagram.	[8]
	b)	Give the block diagram of NE 565 PLL and explain the role of each block. Explain how PLL is used as FM demodulator?	[7]
5	a)	Explain the operation of an all pass filter with its circuit diagram. Also determine the phase shift Φ between the input and output at f=2KHz. To obtain a positive phase shift 'Φ' what modifications are necessary in the circuit?	[7]
	b)	Draw circuit diagram and explain the 4-bit weighted resistor type D/A converter in detail. What are the limitations of weighted resistor type D/A converter?	[8]
6	a)	Distinguish between encoder and a decoder.	[4]
	b)	Draw the circuit of a 3 to 8 decoder and explain its operation. How this can be used as a DEMUX.	[6]
	c)	Design a full-subtractor using 3:8 decoders.	[5]
7	a)	Design a modulo -16 synchronous binary counter using T- flip flops.	[8]
	b)	Design Johnson counter with ten timing signals.	[7]
8	a)	What is a PROM? What are the advantages and disadvantages of using a PROM as a PLD?	[8]
	b)	Explain with suitable diagrams, the structure of a DRAM cell.	[7]

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