Code No: RT32042 **R13** SET - 1

III B. Tech II Semester Regular Examinations, April - 2016

DIGITAL SIGNAL PROCESSING

(Electronics and Communication Engineering)

Time: 3 hours Maximum Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Find the power of the given signal below? [4M]

$$x[n] = \begin{cases} 3(-1)^n, & n \geq 0 \\ 0 & n < 0 \end{cases}$$

b) Compare overlap-add method and overlap-save method [4M]

c) Compare direct form I and direct form II realization of IIR systems. [4M]

d) What conditions are to be satisfied by the impulse response of an FIR system in order to have a linear phase? [3M]

e) What is the need for multirate signal processing? [3M]

f) What are the differences between fixed type processors and floating type processors? [4M]

PART –B

2 a) Find the solution to the following linear constant coefficient difference equation [10M]

$$y(n) - \frac{3}{2}\, y\,(n-1) + \frac{1}{2} y(n-2) = \left(\frac{1}{2}\right)^n \; for \; n \geq \; 0$$

With initial conditions y(-1) = 4 and y(-2) = 10.

b) Derive the relationship between impulse response and frequency response of a discrete time system. [6M]

3 a) Compute the DFT of the sequence x(n) = sin[nπ/4], where N=8 using DIT FFT algorithm [8M]

b) Determine the IDFT of the sequence [8M]

$$X(K) = (6, -\sqrt{2} - j4.8284, -2 + j2, \sqrt{2} - j0.8284, -2, \sqrt{2} + j0.8284, -2 - j2, -\sqrt{2} - j4.8284$$

4 Obtain the cascade and parallel realisation structures for the following signals. [16M]

$$H(z) = \frac{2(1 - z^{-1})(1 + \sqrt{2}z^{-1} + z^{-2})}{(1 + 0.5z^{-1}(1 - 0.9z^{-1} + 0.81z^{-2}))}$$

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5 a) The desired frequency response of a low pass filter is

$$H_d(e^{jw}) = \begin{cases} e^{-j3w} & \frac{-3\pi}{4} \le w \le \frac{3\pi}{4} \\ 0 & elsewhere \end{cases}$$

[10M]

Determine $H(e^{jw})$ for M =7 using a rectangular window.

b) What are the effects of windowing? [6M]

6 a) Derive an expression for the spectrum of output signal of an decimator. [8M]

b) What are the applications of multirate system? [8M]

7 a) What is MAC? Explain its operation in detail. [10M]

b) What are the various addressing modes used in the TMS320C5X processor? [6M]

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3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Show that the following systems are nonlinear and time invariant. [4M]
y(n) – x(n)y(n-1) = x(n)

b) Write computation efficiency of FFT over DFT. [3M]

c) What are the basic building blocks of realization structures? [4M]

d) Obtain the mapping formula for the impulse invariant transformation. [4M]

e) Write some examples of multirate digital systems. [3M]

f) What are the advantages of DSP processors in relation to general purpose processors? [4M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]

$$y(n) - \frac{1}{2}y(n-1) = x(n)$$

b) Explain causality and stability of a linear time invariant system. [6M]

3 a) Find the DFT of the following sequence using FFT DIF? [8M]
X(n) = {1,2,3,5,5,3,2,1}

b) Compute the DFTs of the sequence $x(n) = 2^{-n}$, where N = 8 using DIT algorithm [8M]

4 Develop the cascade and parallel forms of the following causal IIR transfer functions. [16M]

$$H(z) = \frac{(3 + 5z^{-1})(0.6 + 3z^{-1})}{(1 - 2z^{-1} + 2z^{-2})(1 - z^{-1})}$$

5 a) Convert the analog filter to a digital filter whose system function is [10M]

$$H(s) = \frac{1}{(s+2)^2 + (s+1)}$$

Use bilinear transformation.

b) What is a Kaiser window? In what way is it superior to other window functions? [6M]

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6 a) Draw the block diagram of a multistage interpolator and explain it [8M]

b) A one stage decimator is characterized by the following Decimator factor = 3. Anti-aliasing filter coefficients h(0) = -0.06 = h(4), h(1)=0.3 =h(3), h(2) =0.62. Given the data, s(n) with successive values [6,-2,-3,8,6,4,-2], calculate and list the filtered output and the output of the decimator [8M]

7 a) Draw and explain the memory architecture of the TMS320C3X processor. [10M]

b) What are the major advantages of having on-chip memory? [6M]

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Time: 3 hours Maximum Marks: 70

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1 a) Show that the following system is nonlinear and time invariant. [4M]
y(n+2) +2y(n) = x(n+1) +2

b) State all properties of DFT [4M]

c) Distinguish the canonic and non-canonic structures. [4M]

d) Discuss the stability of the impulse invariant mapping technique. [3M]

e) What is meant by aliasing? How to avoid it? [4M]

f) List the basic characteristics of digital signal processor. [3M]

PART –B

2 a) Determine the frequency response, magnitude and phase responses and time delay of the systems given by [10M]
y(n) = x(n) – x(n-1) + x(n - 2)

b) State and explain the transfer function of an LTI system. [6M]

3 a) Find the N-point DFT for x(n) = a^n for 0 < a < 1? [8M]

b) Given x(n) = {1,2,3,4,4,3,2,1}, find X(k) using DIF FFT algorithm. [8M]

4 Realize the following IIR system functions in the direct form I and II and also parallel form. [16M]

$$H(z) = \frac{1}{(1 + az^{-1})(1 - bz^{-1})}$$

5 a) Design a digital Butterworth filter that satisfies the following constraint using bilinear transformation. Assume T=1sec. [10M]

$$0.9 \le \left|H(e^{jw})\right| \le 1 \qquad 0 \le w \le \frac{\pi}{2}$$

$$\left|H(e^{jw})\right| \le 2 \qquad \frac{3\pi}{4} \le w \le \pi$$

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b) What is a Hamming window function? Obtain its frequency domain characteristics. [6M]

6 a) Draw the block diagram of a multistage decimator and explain it [8M]

b) Discuss the computationally efficient implementation of decimator in an FIR filter. [8M]

7 a) Draw and explain the major block diagram of the TMS320C3X. [10M]

b) Explain the function of Barrel Shifter in the digital signal processor. [6M]

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2. Answering the question in **Part-A**is compulsory
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1	a)	What is BIBO stability? What are the conditions for BIBO system?	[4M]
	b)	How FFT is more efficient to determine DFT of sequence?	[3M]
	c)	Distinguish between the methods of realization namely, block diagram representation and signal flow graph for implementing the digital filter transfer function.	[4M]
	d)	What is the impulse invariant technique?	[4M]
	e)	What are the drawbacks in multistage implementation?	[3M]
	f)	Mention various generations of digital signal processors.	[4M]

PART –B

2	a)	Determine frequency, magnitude and phase responses and time delay for the system. $$y(n) + \frac{1}{4}y(n-1) = x(n) - x(n-1)$$	[10M]
	b)	Define the terms : linearity, time invariance and causality for a discrete time system.	[6M]
3	a)	Compute the FFT for the sequence x(n) = n+1 where N =8 using DIT algorithm	[8M]
	b)	State and prove the periodicity property in DFT.	[8M]
4		Realize the following IIR system functions in the direct form I and II and also parallel form. $$H(z) = \frac{1}{(1-az^{-1})^2} + \frac{1}{(1-bz^{-1})^2}$$	[16M]
5	a)	What are the requirements for converting a stable analog filter into a stable digital filter?	[6M]

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b) The desired frequency response of a low pass filter is [10M]

$$H_d(e^{jw}) = \begin{cases} 1; & \frac{-\pi}{2} \le w \le \frac{\pi}{2} \\ 0; & \frac{\pi}{2} \le w \le \pi \end{cases}$$

Determine $h_d(n)$ for M =7 using a rectangular window.

6 a) How can sampling rate be converted by a rational factor M/L? [8M]

b) Draw and explain the polyphase structure of a interpolator. [8M]

7 a) Explain the purpose of six registers used in the TMS320C2X processor. [10M]

b) What are the limitations of pipelining in Digital Signal Processor? [6M]

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