Code No: R21054 **R10** SET - 1

II B. Tech I Semester Supplementary Examinations, May/June - 2017
DIGITAL LOGIC DESIGN
(Com. to CSE, IT)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Convert the following to decimal and then to octal. (8M)
   i) $(4234)_{16}$ ii) $(125F)_{16}$ iii) $(10010011)_2$ iv) $(10111111)_2$
   b) Represent the decimal number 6027 in (7M)
   i) BCD ii) excess-3 Code iii) 2 4 2 1 Code

2. a) Draw the logic symbol, expression and truth table for following logic gates: (8M)
   i) AND ii) OR iii) NOT iv) NAND v) NOR vi) EX-OR vii) EX-NOR
   b) Realize the EX-OR Operation with minimum number of NAND gates (4M)
   c) Simplify the Boolean function xy+x'z+yz to a minimum number of literals. (4M)

3. a) What do you mean by K-map? Draw 3-variable K-map and define pair, quad and octet. (8M)
   b) Simplify the Boolean function F (w, x, y, z) = Σ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) using K-map. (7M)

4. a) Design a circuit to eliminate the propagation delay in the parallel adder. (7M)
   b) Design an 8-bit adder using two 74LS283s. (8M)

5. Implement the following multiple output combinational logic circuit using a 4-line to 16-line decoder. $f_1 = \Sigma m(1,2,4,7,8,11,12,13)$, $f_2 = \Sigma m(2,3,9,11)$ $f_3 = \Sigma m(10,12,13,14)$ $f_4 = \Sigma m(2,4,8)$ (15M)

6. a) Design BCD to Excess-3 converter using PAL. (8M)
   b) Implement a full subtractor using ROM. (7M)

7. a) Draw the logic diagram of an SR latch with control input using NAND gates. (6M)
   b) Draw the circuit of master-slave JK flip-flop and explain its operation with the help of truth table. (9M)

8. Draw a block diagram of modulo 10 ripple counter and explain its timing. (15M)
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