Code No: R1621053 **R16** SET - 1

II B. Tech I Semester Regular/Supplementary Examinations, October/November - 2018
DIGITAL LOGIC DESIGN
(Com to CSE & IT)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Write the difference between combinational circuit and sequential circuit (2M)
   b) A computer has a word length of 9 bits including sign. If 2's complement is used to represent negative numbers, what range of integers can be stored in computer? Express your answer in hexadecimal. (3M)
   c) Factor the following expression to obtain a product of sums XY+Z'W' (2M)
   d) Draw 4-variable K-map and define pair, quad and octet. (3M)
   e) Draw the circuit represented by the following VHDL statements: (2M)
   W<=X and Y;
   X<=U or P;
   U<=Q and R;
   P<= not S and T;
   f) Distinguish between Moore and Mealy Machines. (2M)

PART -B

2. a) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation. (8M)
   b) Perform the subtraction using 2's complement method. (6M)
   (i)11010 – 10100 (ii)11010 – 1101.10 (iii)110 - 110000

3. a) Simplify each of the following expressions (6M)
   i) ab +a'bc' +bc
   ii)(ab' +c) (a +b')c
   iii)ab' +c +(a'+b)c'
   b) Find both the Minterm expansion and Maxterm expansion for the following function using algebraic manipulations (8M)
   f (X,Y,Z,W) =XY +X'ZW

4. a) Find the minimum sum-of-products expression for (6M)
   f (x,y,z,w) =∑ m (1,2,4,15) +∑ d(0,3,14) using K -map
   b) Make a K-map for the function (8M)
   f (x,y,z,w) =xy +xz' +z +xw +xy'z +xyz and realize the minimized expression using NAND gates only

5. a) Design and draw a full adder which will use two half adders. (7M)
   b) Define decoder. Construct 3x8 decoder using logic gates . (7M)
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6. a) Design a SR flip flop using NAND gates. Explain the operation of the SR flip flop with the help of characteristic table. (7M)
   b) Draw the diagram of Mealy type FSM for serial adder (7M)

7. a) Design a mod-11 Ripple counter using T flip flops and explain its operation with the help of the state diagram (7M)
   b) Explain the operation of 4-bit ring counter with circuit diagram and timing diagrams. (7M)

Code No: R1621053 **R16** SET - 2

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Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Write the difference between Synchronous and asynchronous circuits (2M)
   b) A computer has a word length of 9 bits including sign. If 1's complement is used to represent negative numbers, what range of integers can be stored in computer? Express your answer in hexadecimal. (3M)
   c) Multiply out and simplify to obtain a sum of products :
   (x' +y +z') (x' +z' +u) (y' +u') (2M)
   d) Realize the2 input X-OR gate using minimum number of NAND gates (3M)
   e) Draw the circuit represented by the following VHDL statements: (2M)
   W<=X or Y;
   X<=U and P;
   U<=Q and R;
   P<= not S and T;
   f) Write the excitation table for S-R and T flip-flops. (2M)

PART -B

2. a) The solution to the quadratic equation $x^2 - 11x + 22 = 0$ is x = 3 and x = 6. What is the base of numbers. (8M)
   b) Perform the subtraction using 1's complement method. (6M)
   (i)11010 – 10000.01 (ii)11010 – 1101 (iii)101 - 110000

3. a) Simplify each of the following expressions (6M)
   i) w'x' +x'y' +yz +w'z'
   ii)xy +x'yz' +yz
   iii)x'w(y' +z) +x'w' (y +z') +(y' +z)(y +z')
   b) Find both the Minterm expansion and Maxterm expansion for the following function using algebraic manipulations (8M)
   f (X,Y,Z,W) =(X +Y+W') (X' +Z) (Z +W)

4. a) Find the minimum sum-of-products expression for (6M)
   f (x,y,z,w) =∏M (0,1,2,5,7.9.11) .∏ D(4,10,13) using K -map
   b) Make a K-map for the function (8M)
   f (x,y,z,w) =(x+y) (x+z') z (x+w)(x+y'+z) (x+y+z) and realize the minimized expression using NOR gates only

5. a) Design and draw a full subtractor which will use two half subtractors. (7M)
   b) Define multiplexer. Construct 4-to-1 multiplexer using logic gates (7M)
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Code No: R1621053 **R16** SET - 2

6. a) Design a SR flip flop using NOR gates. Explain the operation of the SR flip flop with the help of characteristic table. (7M)
   b) Draw the diagram of Moore type FSM for serial adder (7M)

7. a) Design a mod-14 Ripple counter using T flip flops and explain its operation (7M)
   b) Explain the operation of 4-bit twisted ring counter with circuit diagram and timing diagrams. (7M)

Code No: R1621053 **R16** SET - 3

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Represent +43 and -43 in sign magnitude, sign 1's complement and sign 2's Complement representation (3M)
   b) State and prove the DeMorgan's laws. (2M)
   c) Prove that NOR gate is an universal gate. (2M)
   d) Implement the following VHDL conditional statement using two 2 -to- 1 MUX es:
   Z< = X when U ='1' else Y when V ='1' else W ; (2M)
   e) Write the excitation table for D and T flip-flops. (2M)
   f) Draw the diagram of three bit ring counter and give its state diagram (3M)

PART -B

2. a) Solve the following (8M)
   i) $(57.125)_{10}$ = ( )$_8$
   ii) $(30.6875)_{10}$ = ( )$_2$
   iii) $(137.75)_8$ = ( )$_{10}$
   b) Perform the subtraction using 1's complement method. (6M)
   (i)11010 – 10010.01 (ii)11010.01 – 1101 (iii)101 - 110000

3. a) Simplify each of the following expressions (6M)
   i) (a+b) (a'+b+c') (b+c)
   ii)(a+b') c+ a b'+c
   iii)a +a'b +a'b'c +a'b'c'd+.....
   b) Find both the minterm expansion and maxterm expansion for the following function using algebraic manipulation (8M)
   f (X,Y,Z,W) =X YW'+ X' Z + ZW

4. a) Find the minimum product-of sums expression for (6M)
   f (x,y,z,w) =$\sum$ m (0,3,4,15) +$\sum$ d(1,2,14) using K -map
   b) Make a K-map for the function (8M)
   f (x,y,z,w) =xz +xz' +w+xy'+xy'z +xyz and realize the minimized expression using NAND gates only

5. a) Realize the function f(A,B,C,D) = $\sum$ (1,2,3,4,6,7,8,10,12,14,15) using (7M)
   i) 8:1 MUX ii) 4:1 MUX
   b) Perform the realization of half adder and full adder using decoders and logic gates (7M)
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Code No: R1621053 **R16** SET - 3

6. a) Design a SR flip flop using NAND gates. Explain the operation of the SR flip flop with the help of characteristic table and characteristic equation. (7M)
   b) With simple examples explain the differences between Mealy and Moore type machines (7M)

7. a) What are the different types of registers? Explain the Serial Input Serial Output shift register (7M)
   b) Design a 4-bit binary UP/DOWN ripple counter with a control for UP/DOWN counting. (7M)

Code No: R1621053 **R16** SET - 4

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2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1. a) Represent +53 and -53 in sign magnitude, sign 1's complement and sign 2's Complement representation (3M)
   b) State and prove the Consensus theorem. (2M)
   c) Prove that NAND gate is an universal gate (2M)
   d) Implement the following VHDL conditional statement using two 2 -to- 1 MUXes:
   Z< = Y when U ='1' else X when V ='1' else W ; (2M)
   e) Write the characteristic equation for S-R flip-flop (2M)
   f) Draw the diagram of three bit twisted ring counter and give its state diagram (3M)

PART -B

2. a) Solve the following (8M)
   i) $(87.125)_{10}$ = ( )$_{16}$
   ii) $(37.6875)_{10}$ = ( )$_{8}$
   iii) $(147.75)_{8}$ = ( )$_{10}$
   b) Perform the subtraction using 2's complement method. (6M)
   (i)11010 – 10001.01 (ii)11010 – 1101 (iii)101.01 - 110000

3. a) Simplify each of the following expressions (6M)
   i) (w'+x') (x'+y') (y+z) (w'+z')
   ii)(x+y) (x'+y+z') (y+z)
   iii)x'w(y' +z) +x'w' (y +z') +(y' +z)(y +z')
   b) Find both the minterm expansion and maxterm expansion for the following function using algebraic manipulation (8M)
   f (X,Y,Z,W) =(X+Y) (X'+Z+W)

4. a) Find the minimum product - of sums expression for (6M)
   f (x,y,z,w) =∏M (0,1,2,4,7.9.10) .∏ D(5,11,13) using K -map
   b) Make a K-map for the function (8M)
   f (x,y,z,w) =(x+y) (x+z')w (x+w)(x+y'+z) and realize the minimized expression using NOR gates only

5. a) Realize the function f(A,B,C,D) = ∑ (0,2,4,6,7,8,9,10,13,15) using (7M)
   i) 16:1 MUX ii) 8:1 MUX
   b) Design a 4 bit ADDER/SUBTRACTOR circuit with add/sub control line (7M)
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Code No: R1621053 **R16** SET - 4

6. a) Design a JK flip flop using AND gates and NOR gates. Explain the operation of the JK flip flop with the help of characteristic table and characteristic equation (7M)
   b) Write the capabilities and limitation of finite state machines. (7M)

7. a) What are the different types of registers? Explain the Parallel Input Serial Output shift register (7M)
   b) Design a 3 bit counter which counts in the sequence: 001,011,010,110,111,101,100..(repeat). Use S-R flip-flops. (7M)