Code No: R1622023 **R16** SET - 1

II B. Tech II Semester Regular Examinations, April - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Electrical and Electronics Engineering)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	What are the three methods of obtaining the 2's complement of a given binary number?	(3M)
	b)	What do you mean by K-map? Name it advantages and disadvantages.	(3M)
	c)	Distinguish between a half-adder and a full-adder?	(2M)
	d)	What is a PLD? What is the principal advantage of a PLD?	(2M)
	e)	Draw the state diagram of modulo-4 up/down counter.	(2M)
	f)	By how many models are synchronous sequential circuits represented? Name them.	(2M)

PART -B

2.	a)	Find the 12-bit 1's complement form of the following decimal numbers. i) -97 ii) -224 iii) -205.75 iv) -29.375	(7M)
	b)	Without reducing, implement the following expressions in AOI logic and then convert them into NAND logic and NOR logic i) A + BC + (A + B'C) + D ii) A + B'C + (B + C)' + B'C'	(7M)
3.	a)	Obtain the minimal expression using the tabular method F = πM (6, 7, 8, 9). d (10, 11, 12, 13, 14, 15)	(7M)
	b)	Simplify the following Boolean expression. T(x, y, z) = (x + y) {[x' (y' + z')]'} +x' y' +x' z' X(A, B, C, D) = $A^1B^1C^1$+(A+B+C^1)^1+$A^1B^1C^1$D	(7M)
4.	a)	Draw the logic diagram of a 2 to 4 line decoder using NOR gates including an enable input.	(7M)
	b)	Give circuit implementation of 4 Bit Ripple adder and Ripple Adder/Subtractor using ones and twos complement method.	(7M)
5.	a)	Design an arithmetic circuit that adds 2 binary digits. The circuit should have 2 outputs, one for the sum and the other for the carry. Implement the same in a PAL.	(7M)
	b)	Show how the PLA circuit can be programmed to implement the binary to gray conversion.	(7M)
6.	a)	Draw the schematic circuit of a D flip flop with negative edge triggering using NAND gates. Give its truth table and explain its operation?	(7M)
	b)	What is a register? Discuss the applications of shift registers?	(7M)
7.	a)	With suitable example explain the Mealy and Moore models?	(7M)
	b)	Explain the terms state diagram and state table with suitable example.	(7M)
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PART –A

1. a) Convert the following numbers with the given radix to decimal. (3M)
   i. 4433_5 ii. 1199_{12}
   b) State and prove De Morgan's theorem. (3M)
   c) Define encoder? List out the applications of it? (2M)
   d) What are the advantages of PLDs over fixed function ICs? (2M)
   e) Explain the operation of a SR flip-flop? (2M)
   f) What is the mealy machine? (2M)

PART -B

2. a) Perform the subtraction using 1's complement and 2's complement methods. (7M)
   i) 11010 – 10000 ii)11010 – 1101 iii)100 - 110000
   b) How are negative numbers represented? Represent signed numbers from +7 to -8 using different ways of representation. (7M)

3. a) Reduce using mapping the following expression and implement the real minimal expression in Universal logic. F= ∑m (0, 2, 4, 6, 7, 8, 10, 12, 13, 15) (7M)
   b) State and prove consensus theorem? Solve the given expression using consensus theorem. (7M)
   (i) $\overline{AB} + AC + \overline{BC} + \overline{BC} + AB$
   (ii) $(A + B)(\overline{A} + C)(B + C)(\overline{A} + D)(B + D)$

4. a) Perform the realization of half adder and full adder using decoders and logic gates. (7M)
   b) Design a combinational logic to subtract one bit from the other. Draw the logic diagram using NAND and NOR Gates. (7M)

5. a) Discuss how PROM, EPROM and EEPROM technologies differ from each other. (7M)
   b) Implement the following multiple output functions using PROM (7M)
   F_1= ∑m (0, 1, 4, 7, 12, 14, 15) F_3= ∑m (2, 3, 7, 8, 10)
   F_2= ∑m (1, 3, 6, 9, 12) F_4= ∑m (1, 3, 5)

6. a) Draw the circuit diagram of a positive edge triggered JK flip flop and explain its operation with the help of a truth table? (7M)
   b) Convert a D flip flop into SR flip flop and JK flip flop? (7M)

7. a) Draw the state diagram for multiplier and implement the corresponding state machine model. (7M)
   b) Explain the state minimization procedure with the help of example. (7M)
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PART –A

1. a) Express the Decimal Digits 0-9 in 8 4 -2- 1. (3M)
   b) Why is minimization of switching functions required? (3M)
   c) Realize a single bit comparator? (2M)
   d) What are the advantages and disadvantages of using a PROM as a PLD? (2M)
   e) Draw and explain active low S-R latch. (2M)
   f) What is the Moore machine? (2M)

PART -B

2. a) Convert the following to Decimal and then to octal (7M)
   (a) $(125F)_{16}$ (b) $(10111111)_2$ (c) $(392)_{10}$
   b) How do you convert a gray number to binary? Generate a 4-bit gray code directly using the mirror image property? (7M)

3. a) What are the limitations of K-maps? Compare K-map and tabular methods of minimization. (7M)
   b) Represent and draw the following Boolean function using minimum number of basic gates. i) (AB + AB') (AB)' (7M)
   ii) [(ABD(C + D + E)) + (A +DBC)'] (ABC + (CAD)')
   iii)

4. a) Realize the function f(A,B,C,D) = $\sum$ (1,2,5,8,10,14)+d (6,7,15) using (7M)
   i) 8:1 MUX ii) 4:1 MUX
   b) Design and draw the logic circuit diagram for full adder/subtractor. Let us consider a control variable w and the designed circuit that functions as a full adder when w=0, as a full subtractor when w= 1. (7M)

5. a) Design a PAL for the following logical functions. (7M)
   Y1=AB+A'CB', Y2=AB'C+AB+AC', Y3=AB+BC+CA
   b) Design a combinational circuit using ROM. The circuit accepts a 3 bit number and generates an O/P binary number equal to square of input number. (7M)

6. a) Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table. (7M)
   b) With suitable logic diagrams explain about Buffer register and Controlled buffer register? (7M)

7. a) Discuss general model of Mealy sequential machine. How do you realize sequential network with a ROM. (7M)
   b) Explain the following with examples: (7M)
   i) Flow table ii) State reduction
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PART –A

1. a) Why is hexadecimal code widely used in digital systems? List out the digits used to represent the hexadecimal codes? (3M)
   b) What is Quine-McClusky method? (3M)
   c) Why a multiplexer is called a data selector? Draw the 2x1 MUX. (2M)
   d) Draw the basic architecture of a PAL? (2M)
   e) What are the various methods used for triggering flip-flops? Explain with examples. (2M)
   f) Compare the Moore and Mealy machines? (2M)

PART -B

2. a) Subtract the following decimal numbers by the 9's and 10's complement methods. (7M)
      i) 274 - 86 ii) 93 - 615 iii) 574.6 - 297.7 iv) 376.3 - 765.6
   b) What is the Hamming code? How is the Hamming code word tested and corrected? (7M)

3. a) State and prove the following laws of Boolean algebra. (7M)
      i) Commutative ii) associative iii) distributive
      iv) idempotence v) absorption
   b) Reduce the following expression to the simplest possible POS and SOP forms. (7M)
      $F = \sum m(6,8,13,18,19,25,27,29,31) + d(2,3,11,15,17,24,28)$

4. a) Implement the following multiple output combinational logic circuit using a 4 line to 16 line decoder: (7M)
      $F_1 = \sum m(0, 1, 4, 7, 12, 14, 15)$ $F_3 = \sum m(2, 3, 7, 8, 10)$
      $F_2 = \sum m(1, 3, 6, 9, 12)$ $F_4 = \sum m(1, 3, 5)$
   b) Discuss a few applications of multiplexers and distinguish between a multiplexer and a decoder. (7M)

5. a) What is a PLD? Compare the three combinational PLDs? (7M)
   b) Design an Excess-3 to BCD code converter using a PLA? (7M)

6. a) Draw the schematic circuit of an edge-triggered JK flip flop with active low preset and active low clear using NAND gates and explain its operation? (7M)
   b) Design a type-D counter that goes through states 0, 2, 4, 6, 0…….. The undesired states must always go to a 0 on the next clock pulse. (7M)
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7. a) For the machine given below find the equivalence partition and a corresponding reduced machine in standard form and also explain the procedure. (9M)

PS	NS,Z X=0	X=1
A	B, 0	E, 0
B	E, 0	D, 0
C	D, 1	A, 0
D	C, 1	E, 0
E	B, 0	D, 0

b) What are the capabilities and limitations of finite state machines? (5M)