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Code No: R1622054 **R16** SET - 1

II B. Tech II Semester Regular Examinations, November - 2018
COMPUTER ORGANIZATION
(Com to CSE, IT, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **FOUR** Questions from **Part-B**

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PART –A

1.	a)	List the functions of system software?	(2M)
	b)	What is interrupt? How the interrupts are processed?	(3M)
	c)	Write about the fetch routine in symbolic microinstructions.	(2M)
	d)	Explain in detail about stored program concept	(3M)
	e)	List out several of characteristics of multi processors.	(2M)
	f)	Define the Inter Process Arbitration.	(2M)

PART -B

2.	a)	With the help of a diagram, review about Arithmetic logic shift unit.	(7M)
	b)	Describe Selective -Set, Selective - Complement, Selective-Clear and mask operation with an example.	(7M)
3.	a)	Draw and illustrate the instruction cycle state diagram.	(7M)
	b)	Represent the decimal number 8620 in (i) BCD; (ii) excess-3 (iii) 2421 code (iv) As a binary number.	(7M)
4.	a)	Arrange the organizations of micro programmed control unit with neat sketch.	(7M)
	b)	Explain the following with respect to stack organization. i) Stack Operations ii) Reverse Polish Notation	(7M)
5.	a)	Distinguish the following mapping functions i) Associative mapping. ii) Direct mapping iii) Set Associative mapping	(14M)
6.	a)	Summarize the following secondary storage devices i) Magnetic disk. ii) Magnetic tape.	(7M)
	b)	Explain how the technique of pegging can be implemented?	(7M)
7.	a)	A two-way set associative cache memory uses blocks of four words. The cache can accommodate a total of 2048 words from main memory .the main memory size is 128K×32. i) Formulate all pertinent information required to construct the cache memory. ii) What is the size of the cache memory?	(7M)
	b)	Write short notes on Arithmetic pipeline	(7M)

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