Code No: R22023 **R10** SET - 1

II B. Tech II Semester Supplementary Examinations, November -2018
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1.	a)	Convert the following decimal numbers to the indicated base: i) 7562.45 to Octal ii) 1938.257 to hexadecimal iii)175.175 to binary	(7M)
	b)	Perform the subtraction with the following unsigned binary numbers by taking the 2's complement of subtrahend i) 11010 – 10000, ii) 11010 – 1101, iii) 100 – 110000, iv) 1010100 – 1010100	(8M)
2.	a)	Simplify the following Boolean expressions to a minimum number of literals i) ABC+A'B+ABC' ii) x'yz +xz iii) (x +y)'(x' + y')	(8M)
	b)	Determine the single error correcting code for the information code 10111	(7M)
3.	a)	Minimization of function f using K-map f(A,B,C,D) = ∑(0,2,3,4,6,7,8,10) + d(12,13,14,15)	(10M)
	b)	Define prime implicates? What are prime implicates in above expression?	(5M)
4.	a)	Design full subtractor circuit	(5M)
	b)	Design BCD code to excess-3 code converter circuit	(10M)
5.	a)	Draw the logic diagram of 8 to 3 line encoder using three 4 input NAND gates	(8M)
	b)	Design full adder using 3 to 8 decode block	(7M)
6.	a)	Write the merits of PROM,PLA and PAL	(5M)
	b)	A combinational circuit is defined by the functions $F_1(A,B,C) = \sum(3, 5, 6, 7)$ $F_2(A,B,C) = \sum(0, 2, 4, 7)$ Implement the circuit with PROM	(10M)
7.	a)	With the aid of external logic, convert D type flip-flop to a JK flip-flop.	(8M)
	b)	Explain about universal shift register	(7M)
8.	a)	What is a sequence detector? Draw the state diagram of sequence detector which can detect 1011	(5M)
	b)	The output Z of a fundamental mode, two input sequential circuit is to change from 0 to 1 only when x2 changes from 0 to 1 while x1=1. The output changes from 1 to 0 only when x1 changes from 1 to 0 while x2=1. Find a minimum row reduced flow table	(10M)
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