Code No: RT22022 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, November - 2018
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Convert the following: i) $(A61)_6 = (\ )_{10}$, ii) $(1266)_8 = (\ )_{16}$
   b) Obtain the complement of the following Boolean expressions.
   i) AB+A(B+C)+B'(B+D) ii) A+B+A'B'C
   c) What are the advantages and disadvantages of the tabular method when compassed to the K-map?
   d) Write short notes on ROM, PAL and PLA.
   e) Write short notes on RS Flip Flop using NAND gates.
   f) Write a short notes on ROM.

PART -B

2. a) Perform the following binary arithmetic operations using 1's complement and 2's complements. i) 1101.1101-1011.10 ii) $(642)_8$ -- $(530)_8$.
   b) Construct a seven-bit error-correcting code to represent the decimal digits by augmenting the excess-3 code and by using odd-1 parity check.

3. a) Simplify the following Boolean expressions to a minimum number of literals.
   i) $A^1B(D^1 + C^{1}{}'D) + B(A + A^1CD)$.
   ii) $(x^1 y^1 + z)^1 + z + xy + wz$.
   b) Simplify the following function using Karnaugh map method.
   $f = \Sigma m\ (4, 5, 7, 12, 14, 15) + \Sigma d\ (3, 8, 10)$.

4. a) Briefly explain the design and operation of a carry look ahead adder.
   b) Construct a 5 x 32 decoder with four 3 x 8 decoders and one 2 x 4 decoder.
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5. a) Write short notes on ROM, PAL and PLA
   b) Implement following four Boolean functions using ROM and PLA.
   i) $f_1(A,B,C) = \Sigma(1, 2, 4, 6)$. ii) $f_2(A,B,C) = \Sigma(0, 1, 6, 7)$.
   iii) $f_3(A,B,C) = \Sigma(2, 6)$. iv) $f_4(A,B,C) = \Sigma(1, 2, 3, 5, 7)$.

6. Design a 4 bit universal shift register which can be used as a parallel in- parallel out register, serial in serial out register, serial in - parallel out and parallel in serial out register with a shift option to wards left or right. Explain each of the behavior with timing waveform.

7. a) Define state equivalence and machine equivalence with reference to sequential machines
   b) Derive the state diagram for an FSM that has an input w and an output z. The machine has to generate z=1, when the previous four values of w, were 1001 or 1111 otherwise z=0. Overlapping input patterns are allowed.
   An example of the desired behavior is w = 010111100110011111,
   z = 000000100100010011