Code No: R22023   **R10**   SET - 1

II B. Tech II Semester Supplementary Examinations, April-2018
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours   Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1.	a)	Subtract the following numbers using 2's and 1's complement (i) 5250 – 321 (ii) 753 – 864 (iii) 3570 – 2100 (iv) 20 – 1000	[8M]
	b)	Explain about weighted and non-weighted codes	[7M]
2.	a)	Simplify the following Boolean expressions to a minimum number of literals i)ABC+A'B+ABC' ii)x'yz +xz iii) (x +y)'(x' + y')	[8M]
	b)	Implement the following function with NAND gates F(x , y) = Σ(0,3)	[7M]
3.	a)	Simplify the following using QM Tabular Method F(A , B , C , D , E) = Σ(0, 2, 4, 6, 9, 11, 13, 15, 17, 21, 25, 27, 2, 31)	[7M]
	b)	Minimize the given 5 variable function using K-map method f = Σ (3, 4, 9, 10, 11, 12, 18, 20, 21, 22, 23, 25, 26, 30).	[8M]
4.	a)	Draw and explain about BCD adder circuit Excess3 adder circuit	[7M]
	b)	Draw the logic diagram 4-bit binary adder-subtractor circuit and explain	[8M]
5.	a)	Implement the following Boolean function with a multiplexer (a) F(A, B, C, D) = Σ(1, 2, 5, 8, 6, 10,12,14) (b) F(A, B, C, D) = Σ(1, 2, 5,6, 12)	[8M]
	b)	What is necessity of priority encoder? Explain about 8 to 3 priority encoder.	[7M]
6.	a)	Write the difference between PROM, PLA.	[5M]
	b)	A combinational circuit is defined by the functions $F_1(A,B,C) = \sum(3, 5, 6, 7)$ $F_2(A,B,C) = \sum(0, 2, 4, 7)$ Implement the circuit with a PLA having 3 inputs , four product terms and two output	[10M]
7.	a)	What is flip flop? Explain about JK flip flop.	[8M]
	b)	Explain about universal shift register	[7M]
8.	a)	What is Finite state machine and explain its capabilities	[7M]
	b)	Draw a state diagrams of a sequence detector which can detect 011	[8M]