Code No: RT22054 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, November-2017
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Perform 2's complement Addition, Subtraction between the signed Decimal number +66, -25 using 8 Bit representation (4M)
   b) What is circular shift micro operation (3M)
   c) What are zero address instructions? Explain with the help of an example (4M)
   d) Draw the Booths algorithm flow chart (4M)
   e) Explain about the memory hierarchy (3M)
   f) Explain how to access I/O devices in a system (4M)

PART –B

2. a) Draw the flowchart for adding or subtracting two floating –point binary numbers (8M)
   b) Explain the different types of computers (8M)

3. a) With an example of each, explain memory reference instructions? (8M)
   b) Draw the block diagram of a bus system connected to four register with information transferred serially from any register to any other register. Use a decoder and multiplexer to select the source register and a decoder to select destination register (8M)

4. a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register r1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is
   i) Direct ii) Immediate iii) Relative iv) Register Indirect (8M)
   b) Explain the operation of a Micro programmed control unit using a diagram (8M)

5. a) Multiple $(-7)_{10}$ with $(3)_{10}$ by using Booth's multiplication. Give the flow table of the multiplication (8M)
   b) Draw the circuit of a BCD adder / subtractor and explain its operations (8M)

6. a) The access time of a cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80 percent of the memory requests are for read and the remaining 20 percent for write. The hit ratio for read accesses only is 0.9. A Write-through procedureis used i) What is the average access time of the system considering only memory read cycle? ii) What is the average access time of the system for both read and write requests? iii) What is the hit ratio taking into consideration the write cycles? (10M)
   b) What is virtual memory? With a neat block diagram explain the virtual memory address translation (6M)

7. a) Explain the characteristics of multiprocessors (6M)
   b) Explain about DMA (10M)
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