Code No: R22023 **R10** SET - 1

**II B. Tech II Semester Supplementary Examinations, November-2017**
**SWITCHING THEORY AND LOGIC DESIGN**
(Com. to EEE, ECE, ECC, BME, EIE)

Time: 3 hours Max. Marks: 75

Answer any **FIVE** Questions
All Questions carry **Equal** Marks
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1. a) Explain sign magnitude, 1's complement, 2's complement representation of signed numbers and also give suitable examples for each type. (9M)
   b) Compare the advantages and disadvantages of using sign magnitude and 2's complement representation of signed numbers. (6M)

2. a) Using laws and theorems of Boolean algebra simplify the following; also indicate the law or theorem used at each step. (8M)
   i) (B+D)(A+C) + A(BC + D) ii) XY(Y'Z+ W) + W(X'Y' +X'Y+XY')
   b) Explain in detail the procedure for converting AOI logic into NOR logic using suitable example (7M)

3. Find the essential prime implicants and prime implicants and also all possible minimal expressions for the given function using k-map method. (15M)
   $f = \sum m(1,2,4,5,7,8,10,11,13,14,15,16,18,21,24,27,31)$

4. a) Draw the circuit of a excess-3 adder and explain its operation using examples (8M)
   b) Draw the circuit of a half subtractor using NAND gates and explain its operation in detail using suitable examples. (7M)

5. a) Implement the following functions using suitable size decoder and also draw its sketch (10M)
   $f_1 = \sum m(2,4,7)$, $f_2 = \sum m(1,3,5)$, $f_3 = \sum m(0,2.3,4,7)$
   b) Draw the complete circuit of a 4-to-16 decoder. (5M)

6. a) Implement the following functions using suitable PLA (8M)
   $f_1 = \sum m(0,2,4,6,8,10)$
   $f_2 = \sum m(1,3,5,6,8,10)$
   $f_3 = \sum m(0,1,2.3,9,11,12)$
   b) Implement the following functions using suitable PAL (7M)
   $f_1 = \sum m(0,1,3,5)$
   $f_2 = \sum m(0,3,5,7)$

7. a) Design and realize a 4-bit serial-in-serial-out shift register using JK flip-flop and explain its operation. (8M)
   b) Draw a schematic circuit of a D flip-flop with negative edge triggering using NAND gates and also explain its operation in detail. (7M)

8. a) What is finite state machine, also enlist it's capabilities and limitations. (7M)
   b) Using positive edge triggered JK flip-flops design a 4-bit binary ripple down counter (8M)
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