

Code No: RT22054

R13**SET - 1**

II B. Tech II Semester Supplementary Examinations, April-2018
COMPUTER ORGANIZATION
(Com. to CSE, ECC)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**
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PART -A

1. a) Convert the $(246)_7$ to decimal (4M)
- b) List the phases of instruction cycle (4M)
- c) What are zero address instructions? Explain with the help of an example (4M)
- d) Explain about the array multiplier (4M)
- e) Explain the basic structure of cache memory (3M)
- f) Explain how to access I/O devices in a system (3M)

PART -B

2. a) What is bus? Draw the figure to show how functional units are interconnected using a bus and explain it (8M)
- b) Differentiate between fixed point and floating point representation (8M)
3. a) What is register transfer language? Explain the basic symbols used in register transfer. (8M)
- b) Explain the design of accumulator logic (8M)
4. a) Explain the basic computer instruction formats (8M)
- b) Explain the different types of addressing modes (8M)
5. a) Draw and explain the addition and subtraction of floating point numbers (8M)
- b) Explain the block diagram of BCD adder (8M)
6. a) Explain the block diagram of Associative memory (8M)
- b) Explain about the segmented page mapping (8M)
7. a) Distinguish between Isolated versus Memory Mapped I/O (8M)
- b) Explain about the Daisy chain arbitration (8M)