Code No: RT22022 **R13** SET - 1

II B. Tech II Semester Supplementary Examinations, April-2018
SWITCHING THEORY AND LOGIC DESIGN
(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
2. Answer **ALL** the question in **Part-A**
3. Answer any **THREE** Questions from **Part-B**

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PART –A

1. a) Convert the following to Decimal
   i) $(23111)_6$ ii) $(7667)_8$
   b) Write short note on prime implicant chart
   c) What is a Hazard in a Digital system?
   d) Write short notes on PROM.
   e) Explain about the. J-K Master slave flip flop
   f) Compare Melay and Moore models

PART –B

2. a) Draw the NAND logic diagram that implements the complement of the following function. F(A,B,C,D) = Σ (0,1,2,3,4,8,9,12)
   b) Obtain the complement of the following Boolean expressions.
   i) A'C'+ABC+AC' ii) (x'y'+z)'+z+xy+wz
   iii) A'B(D'+C'D)+B(A+A'CD) iv) (A'+C)(A'+C')(A+B+C'D)

3. Reduce the following function using six variable K- map $F = \Sigma m(0, 2, 5, 7, 9, 11, 14, 16, 18, 21, 23, 27, 30, 32, 34, 36, 41, 43, 44, 48, 50, 52, 53, 59, 60, 61)$.

4. a) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers.
   b) Design a circuit to convert Excess-3 code to BCD code Using a 4-bit Full adder.

5. Write a brief note on:
   i) Architecture of PLDs ii) Capabilities and the limitations of threshold gates.

6. a) What is Flip-Flop? Explain excitation tables of all Flip-flops.
   b) Explain Johnson counter with diagram.

7. a) A clock mode sequential circuit has to provide z=1 whenever the input completes the Sequence of pulses 1010 and overlapping is allowed. Draw the state diagram and obtain minimal state using partition method
   b) Draw the state diagram of mod-8 Up - Down counter in Moore model and obtain its state table.
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