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SET - 1 **R16** Code No: R1631043 III B. Tech I Semester Regular Examinations, October/November - 2018 **DIGITAL IC APPLICATIONS** (Common to Electronics Communication Engineering and Electronics Instrumentation Engineering) Time: 3 hours Max. Marks: 70 Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answer ALL the question in Part-A 3. Answer any FOUR Questions from Part-B PART –A 1. What are the advantages and disadvantages of CMOS technology? a) [2M] Give the program structure. b) [2M] c) What is the difference between if and case statement. [2M] Write a VHDL program for 4x1 multiplexer. d) [3M] What is the difference between Ring Counter and Twisted ring counter? e) [3M] Explain the significance of State Reduction. f) [2M] PART -B Explain the terms i) DC noise margin ii) Fan-out with reference to TTL gate. 2. a) [7M] Design CMOS transistor circuit for 3-input AND gate. With the help of function b) [7M] Tables explain the operation of the circuit diagram. Explain the structure of various LOOP statements in VHDL with examples. 3. a) [7M] Explain the difference in program structure of VHDL and any other procedural b) [7M] language. Give an example. Design a 2 to 4 decoder circuit. Give its entity declaration behavioural model. 4. [7M] a) Also draw the waveform giving relation between its inputs and outputs. Explain about variable assignment statement, signal assignment statement, wait b) [7M] statement. Design a 24-bit comparator circuit using 74×682 ICs and explain the functionality 5. a) [7M] of the circuit. Also implement VHDL source code in data flow style. Design and implement counter using VHDL which counts up to 9 and down b) [7M] counts again from 9 to 0. Design a conversion circuit to convert a D flip-flop to J-K flip-flop. Write data-6. a) [7M] flow style VHDL program. Draw the circuit of a bidirectional shift register with parallel loading using 2 to 4 b) [7M] line decoder and D-flip-flops. 7. a) What is meant by finite state machine? What are the capabilities and limitations of [7M] finite state machine? b) Write short notes on the following with suitable examples. [7M] i)State diagram ii)State table iii)state assignment *****



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SET - 2

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Time: 3 hours Max. Marks: 70						: 70
		2. A 3. A	Answer ALL the quest Answer any FOUR Q	stion in Part- uestions fron		
		~~~~~	 <u>PA</u>	~~~~~ <u>RT –A</u>	~~~~~	
•	a) b)		evels of CMOS and T ration data type in VF		amples.	[2M] [2M]
	c) d)		ain Loop statement. program for 1 x 4 der	nultiplexer.		[2M] [3M]
	e) f)	-	s State diagram and s	tate table.	synchronous Counters.	[3M] [2M]
				<u>RT -B</u>		[7M]
2.	a) b)	Draw the dynamic electrical behaviour of CMOS inverter and explain. Explain the differences between TTL, ECL & CMOS logic family.				
3.	a) b)	Discuss the binding? Discuss the binding between entity and components. Write a process based VHDL program for the prime-number detector of 4-bit input and explain the flow using logic circuit.				
1.	a) b)	Discuss Inertial Delay Model? Explain the concept of internal logic synthesizer and also draw the schematic.				[7M [7M
5.	a)	With the help of logic diagram explain 74×157 multiplexer. Write the data flow Style VHDL program for this IC?				[7M]
	b)	Explain about Comparator and design a 16-bit comparator using 74×85 IC's. Write VHDL program.				
5.	a) b)	Explain how a JK- flip-flop can be constructed using a T- flip-flop. Write down truth table, VHDL Code for the 4 bit register with parallel load. Also draw the circuit and output waveform.				
7.	a) b)	Explain the minimization of completely specified sequential machines. Convert the following melay machine into a corresponding Moore machine.				[7M] [7M]
		P.S	NS,X=0	Z, X=1		
		А	B,0	E,0		
		В	E,0	D,0		
		С	D,1	A,0		



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SET - 3

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т:"		Engineering)	J.a. 70
Time: 3 hours Max. Marks			
		<ul> <li>Note: 1. Question Paper consists of two parts (Part-A and Part-B)</li> <li>2. Answer ALL the question in Part-A</li> <li>3. Answer any FOUR Questions from Part-B</li> </ul>	
		<u>PART –A</u>	
1.	a)	Give the logic levels and noise margins of TTL families.	[2M]
	b)	Write a VHDL program for 2x4 Decoder.	[2M]
	c)	Define and explain Next statement.	[2M]
	d)	Explain about Barrel Shifter.	[3M]
	e)	List the various IC versions of shift registers.	[3M]
	f)	What is One hot encoding?	[2M]
		PART -B	
2.	a)	Explain the effect of floating inputs on CMOS gate.	[7M]
	b)	Draw the circuit diagram of basic TTL NAND gate and explain the three parts with the help of functional operation.	[7M]
3.	a)	Explain about dataflow design elements of VHDL.	[7M]
	b)	Write a VHDL program for comparing 8 bit unsigned integers.	[7M]
4.	a)	With examples explain the sequential assignment statements.	[7M]
	b)	Discuss Transport Delay Model.	[7M]
5.	a)	Draw the circuit of a 4-bit ripple carry adder circuit and explain how it is different from look-a-head carry circuit. Give the equation for $C_1$ to $C_4$ for a look-ahead carry adder circuit.	[7M]
	b)	Design a 4 to 16 decoder using two 74×138 decoders.	[7M]
6.	a)	Write down the VHDL code of S-R flip flop.	[7M]
	b)	Give a VHDL code for a 4-bit up counter with enable and clear inputs.	[7M]
7.	a)	Draw the logic diagram of Melay model & explore its operation with examples.	[7M]

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## III B. Tech I Semester Regular Examinations, October/November - 2018 DIGITAL IC APPLICATIONS

(Common to Electronics Communication Engineering and Electronics Instrumentation

Engineering) Time: 3 hours Max. Marks: 70 Note: 1. Question Paper consists of two parts (Part-A and Part-B) 2. Answer ALL the question in Part-A 3. Answer any FOUR Questions from Part-B PART -A 1. Explain the term Transition time with respect to CMOS logic. [2M] a) What are the operators available in VHDL? b) [2M] Define and explain assertion statement. c) [2M] Define three state devices. d) [3M] Write short note on Universal Shift Registers.. e) [3M] f) Distinguish between Mealy and Moore Machines. [2M] PART -B 2. Design a CMOS transistor circuit for 3-input AND gate. With the help of a) [7M] function table explain the circuit. What is interfacing? Explain interfacing between low voltage TTL and low b) [7M] voltage CMOS logic. 3. a) Explain about the following i) Packages with syntax ii) Libraries with syntax. [7M] What is the Significance of time dimension in VHDL? Explain its function. b) [7M] Explain about Inside of a logic synthesizer and Give its schematic. 4. a) [7M] Discuss about Signal Drivers. b) [7M] Write a VHDL code for 4-bit Look ahead carry generator. 5. a) [7M] Implement the 32 input to 5 output priority encoder using four 74LS148 & gates. b) [7M] Write down truth table, VHDL Code for the J-K flip flop using behavioural 6. a) [7M] Modelling. Draw the circuit of MOD 16 Down ripple counter with D-flip-flops and explain b) [7M] its operation. 7. Draw the logic diagram of Moore model & explore its operation with examples. a) [7M] Explain the minimization procedure for determining the set of equivalent state of b) [7M] a specified machine M.

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