Code No: RT31044   **R13**   SET - 1

III B. Tech I Semester Supplementary Examinations, May - 2018
DIGITAL SYSTEM DESIGN & DIGITAL IC APPLICATIONS
(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours   Max. Marks: 70

Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B)**
2. Answering the question in **Part-A** is compulsory
3. Answer any **THREE** Questions from **Part-B**
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PART –A

1	a)	What are the requirements of VHDL?	[3M]
	b)	What are levels of Abstraction in VHDL?	[4M]
	c)	What are the commercial ROM types?	[4M]
	d)	Define Fan in and fan out.	[4M]
	e)	What is a floating point encoder? Explain.	[3M]
	f)	Discuss the steps involved in the analysis of sequential circuits?	[4M]

PART -B

2	a)	Explain brief history of VHDL?	[5M]
	b)	Explain the packages and libraries of VHDL?	[8M]
	c)	Explain about concurrent and sequential statements?	[3M]
3	a)	Explain about major Net list formats for design representation	[8M]
	b)	Discuss about VHDL synthesis	[8M]
4	a)	Explain in detail about PROM with an example?	[8M]
	b)	With the help of logic diagram explain the function of PAL with one example?	[8M]
5	a)	Explain the terms: (i) DC noise margin (ii) Fan-out with reference to TTL gate?	[8M]
	b)	Briefly list out the differences between ECL, TTL and CMOS logic family?	[8M]
6	a)	Design a two bit comparator circuit and explain its operation?	[3M]
	b)	Design a 32x1 multiplexer by sing 74x151 IC and explain its operation?	[8M]
7	a)	With a neat sketch explain the Universal shift rgister	[8M]
	b)	Design MOD-16 synchronous counter using T- Flip-Flop?	[8M]

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