Code No: **R32043** **R10** **Set No. 1**

III B.Tech II Semester Supplementary Examinations, November - 2018

DIGITAL SIGNAL PROCESSING

(Common to Electronics and Communication Engineering and Electronics and Computers Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks

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1 a) Check whether the following systems are linear , causal and time variant [8M]
i) $y(n) = n^2x(2n)$ ii) $y(n) = x^2(n) + x(n-3)$
b) Find the DTFT of $x(n) = a^n u(n)$.Plot $|x(\omega)|$ and $\angle\ x(\omega)$ for a = 0.9 [7M]

2 a) Find convolution of $h(n) = \{1, -3, 5\}$ and $x(n) = \{-1, 4, 7, 3, -2, 9, 10, 12, -5, 8\}$ [8M]
b) Prove the Parseval's theorem for Discrete Fourier Series. [7M]

3 a) By showing all the intermediate results, compute the 8-point DFT of the sequence using DIF FFT algorithm: $y(n) = \{0.5, 0.5, 0.5, 0.5, 0, 0, 0, 0\}$ [8M]
b) Explain DIT-FFT algorithm for the computation of DFT 4-point sequence and List the advantages of FFT. [7M]

4 a) Define *Z*- transform and give the relation between *Z & Laplace* Transforms. Define **ROC** and give some of its properties. [8M]
b) Give the block diagram representation of linear constant coefficient difference equations [7M]

5 a) Explain about design procedure for low pass digital Chebyshev IIR filter [6M]
b) Design a digital Chebyshev IIR low pass filer satisfying the following constraints : [9M]
$0.707 \le |H(w)| \le 1\ ;\ \ 0 \le w \le 0.2\pi$
$|H(w)| \le 0.1;\quad 0.5\pi \le w \le \pi$
Using bilinear transformation and assuming T=1s

6 a) Discuss about frequency sampling technique for FIR filter design. [7M]
b) The desired response of a digital low pass filter is [8M]

$$H_d(e^{jw}) = \begin{cases} e^{-j3w};\ \dfrac{-3\pi}{4} \le |w| \le \dfrac{3\pi}{4} \\ 0\ ;\ \dfrac{3\pi}{4} \le |w| \le 3\pi \end{cases}$$

Determine the filter coefficients and frequency response for N=5 using Hanning window.

7 a) What is the significance of multirate signal processing? Give the applications of multirate signal processing. [8M]
b) What is meant by multistage approach and give the design procedure for Multirate conversion? [7M]

8 a) Draw the block diagram of TMS320C50 DSP processor and explain the functionality of CALU and PLU. [9M]
b) What is the function of Indexed Register and Auxiliary Register? [6M]

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