

Code No: **RT41044**

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IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018 COMPUTER ARCHITECTURE AND ORGANIZATION

(Common to Electronics and Communication Engineering and Electronics and

Instrumentation Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****

PART-A (22 Marks)

1.	a)	What are the data types?	[4]
	b)	Write micro operations for ADD R1, R2.	[3]
	c)	What is sequencer? Mention its functions.	[4]
	d)	Differentiate between static and dynamic memory.	[4]
	e)	What is interrupt?	[3]
	f)	What is pipelining? Draw the diagram for instruction pipelining.	[4]
		PART–B $(3x16 = 48 Marks)$	
2.	a)	Explain error detection with odd parity bit and even parity bit.	[8]
	b)	Explain the bus structures.	[8]
3.	a)	Briefly explain the different instruction formats with suitable examples.	[8]
	b)	Discuss about steps involved in instruction cycle with interrupt enabled.	[8]
4.	a)	Discuss about functioning of micro-programmed control unit.	[8]
	b)	Justify how Hardwired control unit is faster than micro-programmed control unit.	[8]
5.	a)	Draw and Explain about the virtual memory organization.	[8]
	b)	Explain the cache memory mapping techniques.	[8]
6.	a)	What is meant by handshaking? Explain with neat diagram.	[8]
	b)	Explain programmed I/O in detail.	[8]
7.	a)	What is cache coherence problem? Discuss about different cache coherence approaches.	[8]
	b)	Explain briefly about arithmetic pipeline with neat diagram.	[8]

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Set No. 2



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PART-A (22 Marks)

1.	a)	Define and explain Von Neumann Architecture.	[4]
	b)	Define the interrupt cycle.	[3]
	c)	What is microinstruction? Write its format.	[4]
	d)	Draw the memory hierarchy.	[4]
	e)	What is meant by handshaking?	[4]
	f)	What is an arithmetic pipeline?	[3]

<u>**PART-B**</u> (3x16 = 48 Marks)

2.	a)	Give the functional organization of a digital computer and explain the function of	
		each element of a computer.	[8]
	b)	Design a 4-bit adder/subtractor circuit and explain its function.	[8]
3.	a)	Design a digital circuit that performs the four logic operations of AND, OR,	
		Exclusive-OR and NOT. Show the logic diagram of one typical stage.	[8]
	b)	Explain in detail various types of memory –reference instructions with example.	[8]
4.	a)	Explain about microinstruction sequencing techniques, specifically variable format	
		address microinstruction.	[8]
	b)	Explain how control memory functions.	[8]
5.	a)	Explain about virtual memory address translation.	[8]
	b)	Discuss about memory management hardware.	[8]
		S. C.	
6.	a)	What are the different modes of data transfer? Explain each mode in detail.	[8]
	b)	What is Interrupt? Explain the Priority Interrupt technique.	[8]
7.	a)	Discuss in detail about the multiport memory interconnection structure used in	
		multiprocessors.	[8]
	b)	Explain in detail inter processor synchronization.	[8]



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Set No. 3

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Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****

PART-A (22 Marks)

1.	a)	Explain the IEEE single and double precision standard of floating point	
		representation.	[4]
	b)	What are the phases in instruction cycle?	[3]
	c)	Differentiate between hardwired control and micro programmed control unit.	[4]
	d)	Differentiate between RAM and ROM.	[4]
	e)	What are functions of IO processors?	[3]
	f)	What is parallel processing?	[4]
		PART-B $(3x16 = 48 Marks)$	
2.	a)	What are functional units? Discuss on basic functional units of a computer?	[8]
	b)	Derive and explain an algorithm for adding and subtracting 2 floating point	
		binary numbers.	[8]
3.	a)	With examples explain the Data transfer, Logic and Program Control	
		Instructions.	[8]
	b)	Explain the various address modes? Give the suitable examples.	[8]
4.	a)	Discuss the two techniques to design the control unit.	[8]
	b)	List and explain the functions of control unit.	[8]
5.	a)	Explain the memory hierarchy with neat diagram.	[8]
	b)	What is meant by paging? Explain paging technique with an example.	[8]

6. a) Write short notes on I/O devices. b) Explain the strobe control method of asynchronous data transfer.

7.	a)	What is pipelining? Name the two pipeline organizations. Explain about the	
		arithmetic pipeline with the help of an example.	[8]
	b)	Illustrate in detail various characteristics of multiprocessors.	[8]

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Set No. 4



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Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A Answer any THREE questions from Part-B *****

PART-A (22 Marks)

		$\frac{1}{1} \frac{1}{1} \frac{1}$	
1.	a)	Explain the bus structure.	[4]
	b)	What is register transfer language? Give an example for RTL.	[3]
	c)	What is the function of control memory?	[4]
	d)	What is meant by page table?	[3]
	e)	Differentiate between synchronous and Asynchronous modes.	[4]
	f)	Describe the need for Inter Processor Communication.	[4]
		PART-B $(3x16 = 48 Marks)$	
2.	a)	Differentiate between multiprocessor and multicomputer	[8]
	b)	Draw the flowchart for Booth's algorithm for multiplication of signed 2's	[~]
	0)	complement numbers and explain with an example	[8]
			[0]
3.	a)	What is instruction cycle? Explain each phase of instruction cycle with neat	
		diagram?	[8]
	b)	Write about memory read and memory write operations.	[8]
4.	a)	Explain the block diagram of a control unit.	[8]
	b)	Describe micro instruction sequencing with neat block diagram.	[8]
	-)		[]
5.	a)	Explain the Cache memory? Explain how blocks of main memory are addressed	
	/	through the cache blocks.	[8]
	b)	Explain the auxiliary memory.	[8]
	- /	I The second	r.1
6.	a)	With a neat diagram, describe DMA transfer in a computer system.	[8]
	b)	Discuss about Input-output processor.	[8]
	-)		[]
7.	a)	Explain instruction pipeline with neat timing diagram.	[8]
	b)	What is cache coherence problem? Discuss about different cache coherence	r - 1
	- /	approaches.	[8]

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