

Code No: **RT41028****R13****Set No. 1****IV B.Tech I Semester Regular/Supplementary Examinations, Oct/Nov - 2018****VLSI DESIGN****(Electrical and Electronics Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B*

PART-A (22 Marks)

1. a) What is the size of silicon wafer used for manufacturing state-of-the art VLSI IC's? Explain why? [4]
- b) Define Figure of Merit with the necessary expression. [3]
- c) Design a layout diagram for two input nMOS NAND gate. [4]
- d) List and explain the three sources of wiring capacitances. [3]
- e) What are the effects of scaling on V_t ? [4]
- f) Define library. Give the syntax of signal assignment statement. [4]

PART-B (3x16 = 48 Marks)

2. a) Explain the MOS transistor operation with the help of neat sketches in the Depletion mode. [8]
- b) Discuss the steps involved in BiCMOS technology. [8]
3. a) Clearly explain body effect of MOSFET. [8]
- b) Design and draw the circuit diagram of an nMOS inverter and explain its operation with the help of transfer characteristics. [8]
4. a) Design a stick diagram for two input nMOS NOR Gate. [8]
- b) Discuss the transistor related design rule (orbit $2\mu\text{m}$ CMOS). [8]
5. a) Explain in detail about formal estimation of CMOS inverter delay. [8]
- b) Discuss nMOS transistor as a switch. [8]
6. a) Explain the limits of miniaturization on scaling. [8]
- b) In gate logic, compare the geometric aspects between two-input nMOS NAND and CMOS NAND gates. [8]
7. a) List the various abstraction levels in VHDL. Explain any one of them. [8]
- b) Write in brief about logic synthesis process. [8]