

Code No: **PT41046****R13****Set No. 1****IV B.Tech I Semester Supplementary Examinations, February/March - 2018****ADVANCED COMPUTER ARCHITECTURE****(Electronics and Communications Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) Define computer architecture and organization. [4]
- b) Name the four steps in pipelining. [4]
- c) Discuss the limitations of ILP. [3]
- d) Discuss about cross cutting issues. [4]
- e) List the methods for providing synchronization in threads. [4]
- f) Examples of inter connection. [3]

PART-B (3x16 = 48 Marks)

2. a) Discuss Amdahl's law. Explain how to measure and report the performance. [8]
- b) Describe the basic instruction types. Give the control sequence for execution of instruction Add[R3],R1. [8]
3. a) Discuss about the Classic five stage pipe lined RISC processor. [8]
- b) Define pipelining with example and explain its need. [8]
4. a) Explain in detail the steps involved in Tomasulo's algorithm assuming proper data structures. [8]
- b) Explain the complete procedure how hardware supports for exposing more parallelism at compile time? [8]
5. a) What are different forms of parallelism? Explain. [8]
- b) Discuss briefly about the static branch prediction scheme. [8]
6. a) Explain in detail the symmetric shared memory architectures and explain the cache coherence problem in detail. [8]
- b) Discuss briefly about instruction level parallelism. [8]
7. a) Define cluster and discuss designing of clusters in detail. [8]
- b) Explain how the prediction and speculation support will be provided in IA64? [8]