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R13

Set No. 1

IV B.Tech I Semester Supplementary Examinations, February/March - 2018 DIGITAL IC DESIGN

(Electronics and Communications Engineering)

Time: 3 hours

Max. Marks: 70

Question paper consists of Part-A and Part-B Answer ALL sub questions from Part-A

Answer any THREE questions from Part-B

PART-A (22 Marks)

		<u>PARI–A</u> (22 Marks)	
1.	a)	Define Inverter threshold voltage.	[4]
	b)	Explain General circuit structure of an nMOS inverter.	[4]
	c)	Calculate the W/L ratio of the series connected transistors.	[4]
	d)	Discuss about 2 address bits row detector.	[4]
	e)	What is a crosstalk? Explain.	[3]
	f)	State the advantages of Polysilicon Interconnect.	[3]
		$\underline{\mathbf{PART}}_{\mathbf{B}} (3x16 = 48 Marks)$	
2.	a)	Explain necessary theorems of transistor equivalency	[8]
	b)	Derive the expression for gain, input resistance, output resistance of pseudo	
		NMOS inverter.	[8]
3.	a)	Draw and explain the operation of CMOS Transmission gate.	[8]
	b)	Derive the expression for V_{OH} and V_{OL} for two input NOR gate	[8]
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4.	a)	Draw CMOS AOI realization of the JK latch and explain its operation.	[8]
	b)	Discuss how a D Latch can be realized using CMOS.	[8]
		a.	
5.	a)	Explain Domino CMOS Logic gate operation.	[8]
	b)	Discuss the charge-sharing problems in VLSI circuits. Explain various circuit	
		techniques used in domino CMOS circuits for solving charge-sharing problems	[8]
6.	a)	Explain about capacitive interconnect.	[8]
	b)	Estimate the capacitance to ground per unit length for a polysilicon	
		interconnect, 0.25 micro meter wide and 0.25 micrometer thick, on a 0.5 micro	
		meter thick layer of silicon dioxide (relative permitivity = 3.9).	[8]
7.	a)	Draw circuit diagrams of the row decoder and the column decoder for an	
	,	EPROM with 4 rows and 2 columns. Use nMOS technology. Develop formulas	
		for the row and column delays in the EPROM. Define any terms in your	
		formulas which are not obvious.	[12]
	b)	Define memory and give a classification.	[4]

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