Code No: **RT41041** **R13** **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, February/March - 2018

VLSI DESIGN

(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours **Max. Marks: 70**

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A ***(22 Marks)***

1. a) When the channel is said to be pinched –off? [3]
   b) What are the different MOS layers? [4]
   c) Give the different scaling models and scaling factors? [3]
   d) State the disadvantages of dynamic CMOS logic? [4]
   e) What are the different levels of design abstraction at physical design? [4]
   f) What information from the targeted FPGA device is required in RTL synthesis? [4]

PART–B ***(3x16 = 48 Marks)***

2. a) With neat sketches explain the CMOS n-well fabrication process indicating the masks used. [8]
   b) What is threshold voltage of a MOS device and explain its significance. [8]

3. a) Discuss CMOS design style. Compare with nMOS design style? [8]
   b) Design a stick diagram for two input nMOS NAND and NOR gates? [8]

4. a) Why scaling is required? Write the scaling factors for different types of device parameters? [8]
   b) Discuss the limits due to sub threshold currents. [8]

5. a) Describe constructional features and performance characteristic of Pseudo-NMOS logic. [8]
   b) Explain two-phase clock generator using D flip-flops and draw the corresponding waveforms. [8]

6. a) Write down the comparisons between Field Programmable Gate Array and Application Specific Integrated Circuit in detail. [8]
   b) Give the steps in ASIC design flow with flow diagram and briefly discuss about each step. [8]

7. a) Write down the step by step approach of FPGA design process on XILINX environment? [8]
   b) Design a queue and write the dataflow style VHDL program for the same. [8]