Code No: **RT41046**   **R13**   Set No. 1
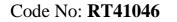
IV B.Tech I Semester Supplementary Examinations, February/March - 2018
ANALOG IC DESIGN
(Electronics and Communication Engineering)

Time: 3 hours   Max. Marks: 70

Question paper consists of Part-A and Part-B
Answer ALL sub questions from Part-A
Answer any THREE questions from Part-B
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PART–A *(22 Marks)*

1. a) Define sheet resistance.   [4]
    b) Define sensititvity of a voltage reference.   [4]
    c) Classify output amplifiers.   [4]
    d) Define slewrate and derive an expression for it.   [4]
    e) What is autozeroing technique?   [3]
    f) Explain how skew reduction is done using PLL.   [3]

PART–B *(3x16 = 48 Marks)*

2. a) Discuss about various capacitances in a MOSFET and derive relation between them.   [8]
    b) Derive the sub threshold MOS model and explain about it.   [8]

3. a) Draw and analyze cascode current mirror.   [8]
    b) Explain about the effect of temperature of voltage references.   [8]

4. a) Explain the operation of active load inverter.   [8]
    b) Using small signal model derive an expression for voltage gain of a differential amplifier.   [8]

5. a) Explain the miller compensation in two stage op-amps.   [8]
    b) Discuss the operation of folded cascade op-amp.   [8]

6. a) What is a comparator? Explain the static and dynamic characteristics of a comparator.   [8]
    b) Find the propagation delay of a open loop comparator having a dominant pole at 10^3rad/s, a DC gain of 10^4, a slewrate of 1V/µS, and a binary output swing of 1V. Assume applied voltage is 10mV.   [8]

7. a) Discuss about non ideal effects in PLL.   [8]
    b) Explain the operation of cross coupled oscillator.   [8]