

Code No: **RT4104B****R13****Set No. 1****IV B.Tech I Semester Supplementary Examinations, February/March - 2018****DIGITAL IC DESIGN****(Electronics and Communication Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) Derive an expression for threshold voltage of an Inverter. [4]
- b) Discuss about the CMOS primitive gates. [4]
- c) Differentiate between flipflop and latch. [4]
- d) Define charge sharing in dynamic gates. [3]
- e) Discuss about Clock Distribution [3]
- f) What are various leakage currents in SRAM cells? [4]

PART-B (3x16 = 48 Marks)

2. a) Explain the operation of a CMOS inverter and derive the expressions for fall and rise times. [8]
- b) Design a pseudo-NMOS logic gate that realizes the function $out = x_1(\bar{x}_2 + x_2x_3)$ Give reasonable dimensions assuming $L_{min} = 0.5\mu m$ [8]
3. a) Explain the operation of a CMOS full adder circuit with neat diagram. [8]
- b) Draw and explain the operation of a 2 input NMOS NAND gate circuit. [8]
4. a) Compare static and dynamic latches. [8]
- b) Draw the logic diagram and truth table of a CMOS clocked SR flip-flop and explain its operation [8]
5. a) List out the different types of issues in CMOS dynamic logic design? Explain anyone with a neat sketch. [8]
- b) Explain the operation of pass transistor logic and explain about leakage and sub threshold currents in dynamic pass gate [8]
6. a) Estimate the low-frequency resistance per unit length for interconnects $0.25\mu m$ wide and $1.0\mu m$ in height made from
 - i) Copper
 - ii) Aluminum
 - iii) N-type polysilicon [8]
- b) Discuss about capacitance interconnect [8]
7. a) Discuss about various leakage currents in SRAM. [8]
- b) With a neat sketch? Explain the principle of NOR gate flash memory. [8]