

Code No: **RT41028****R13****Set No. 1****IV B.Tech I Semester Supplementary Examinations, February/March - 2018****VLSI DESIGN****(Electrical and Electronics Engineering)****Time: 3 hours****Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B*

PART-A (22 Marks)

1. a) Write the limitations of IC's. [3]
- b) Write the problems of Latch-up in CMOS circuits. [4]
- c) What is the need of stick diagrams? [3]
- d) Explain about the constraints in choice of layers. [4]
- e) List out the limitations of scaling. [4]
- f) Write the history of VHDL in brief. [4]

PART-B (3x16 = 48 Marks)

2. a) Why do we use NMOS technology in the design of integrated circuit? [8]
- b) With neat sketches explain how NPN transistors are fabricated in Bipolar process. [8]
3. a) Define the term threshold voltage of MOSFET and explain its significance. [8]
- b) Explain latch-up problem in CMOS circuits. [8]
4. a) Explain procedure for drawing the stick diagram for nMOS design style [8]
- b) Explain in brief about the general observations on the design rules. [8]
5. a) Define and explain the standard unit of capacitance. [8]
- b) Define fan-in and fan-out. Explain their effects on propagation delay. [8]
6. a) Discuss the limits due to sub threshold currents. [8]
- b) Explain clocked CMOS logic and domino logic. [8]
7. a) Discuss the hardware synthesis process. [8]
- b) Classify and explain the digital simulation method. [8]