

Code No: RT22022

R13
SET - 1
II B. Tech II Semester Supplementary Examinations, April/May - 2019
SWITCHING THEORY AND LOGIC DESIGN

(Com. to EEE, ECE, ECC, EIE)

Time: 3 hours

Max. Marks: 70

- Note: 1. Question Paper consists of two parts (**Part-A** and **Part-B**)
 2. Answer **ALL** the question in **Part-A**
 3. Answer any **THREE** Questions from **Part-B**
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PART -A

1. a) What are the Universal gates? Draw the truth tables. 4M
- b) What is a Hazard in a Digital system? 3M
- c) Write short note on prime implicant chart. 4M
- d) List the applications of Multiplexer and Demultiplexer. 3M
- e) Compare synchronous & Asynchronous circuits. 4M
- f) Compare Melay and Moore models. 4M

PART -B

2. a) Convert the following numbers to binary: 9M
 i) $(7EB9)_{16}$ ii) $(7654)_8$ iii) $(525.25)_{10}$
- b) What is the Gray code? What are the rules to construct Gray code? Develop the 4 bit Gray code for the decimal 0 to 15. 7M
3. a) Simplify the following Boolean function using tabular method: 8M
 $f(w, x, y, z) = \sum (2, 6, 8, 9, 10, 11, 14, 15)$
- b) Reduce the following function using K- map and implement it in AOI logic as well as NAND logic. $F = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$ 8M
4. a) Design a 32:1 Multiplexer using two 16:1 and 2:1 Multiplexers. 8M
- b) Design a circuit to convert Excess-3 code to BCD code using a 4-bit Full adder. 8M
5. a) Using PLA logic, implement a BCD to excess 3 code converter. Draw its truth table and logic diagram 8M
- b) Discuss about types of sequential PCDs. 8M
6. a) Distinguish between a state table and a flow table? 8M
- b) Draw the logic diagram and write functional table of an SR latch using NAND gates. Explain the operation. 8M

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7. a) Draw the diagram of mealy type FSM for a serial adder. 8M
b) Reduce the number of states in the following state table and tabulate the reduced state table and give proper assignment. 8M

Present State	Next State , Z	
	X=0	X=1
A	F,0	B,0
B	D,0	C,0
C	F,0	E,0
D	G,1	A,0
E	D,0	C,0
F	F,1	B,1
G	G,0	H,0
H	G,1	A,0