Code No: **RT41041** **R13** **Set No. 1**

**IV B.Tech I Semester Supplementary Examinations, February - 2019**

# VLSI DESIGN

**(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)**

**Time: 3 hours** **Max. Marks: 70**

**Question paper consists of Part-A and Part-B**
**Answer ALL sub questions from Part-A**
**Answer any THREE questions from Part-B**
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## PART–A *(22 Marks)*

1. a) Draw the BICMOS inverter circuit. [4]
   b) Draw the stick diagram of a 2 input NAND gate using CMOS. [4]
   c) Design NAND gate using NMOS technology. [3]
   d) Give the system considerations in subsystem design. [3]
   e) Mention different clocking mechanisms. [4]
   f) Draw basic FPGA design architecture. [4]

## PART–B *(3x16 = 48 Marks)*

2. a) Derive the pull up to pull down ratio for an NMOS inverter. [8]
   b) With neat diagrams, explain the operation of NMOS enhancement mode transistor? [8]

3. a) Explain the various symbols used in stick diagram notation? Draw the stick diagram of CMOS inverter? [8]
   b) Realize the following function F=A XOR B using CMOS logic? [8]

4. a) Derive the propagation delay for NMOS inverter? [8]
   b) Determine the scaling factors of the following:
   (i) Current density (ii) channel resistance (iii) Gate capacitance (iv) Gate delay [8]

5. a) Discuss the clocked sequential circuits for subsystem design. [8]
   b) Explain the architectural issues of subsystem design. [8]

6. a) Discuss the ASIC design flow with neat sketch. [8]
   b) Explain the fault models and stuck at faults. [8]

7. a) Discuss the FPGA configuration and configuration modes. [8]
   b) Explain the modes step by step approach of FPGA design process on Xilinx environment [8]