

Code No: **RT41044****R13****Set No. 1**

IV B.Tech I Semester Supplementary Examinations, February- 2019
COMPUTER ARCHITECTURE AND ORGANIZATION
(Common to Electronics and Communication Engineering and Electronics and Instrumentation Engineering)

Time: 3 hours**Max. Marks: 70***Question paper consists of Part-A and Part-B**Answer ALL sub questions from Part-A**Answer any THREE questions from Part-B************PART-A (22 Marks)**

1. a) What is Mainframe Computer? Write IEEE standard for floating point format. [4]
- b) Give the instruction format of Vector instruction. [3]
- c) What are the advantages and disadvantages of micro programming? [3]
- d) Define the term LRU and LFU. [4]
- e) Explain the significance of cache memory. [4]
- f) Write down the expressions for speedup factor in a pipelined architecture. [4]

PART-B (3x16 = 48 Marks)

2. a) Discuss about Error Detection codes. [8]
- b) State the Non-restoring division technique. [8]
3. a) What are addressing modes? Explain the various addressing modes with examples. [8]
- b) Discuss about logic micro operations. [8]
4. a) Explain the differences between hard wired control and micro programmed control. [8]
- b) Explain how control signals are generated using micro programmed control. [8]
5. a) Discuss the different mapping techniques used in cache memories and their relative merits and demerits. [8]
- b) Discuss about memory management hardware. [8]
6. a) Describe the data transfer method using DMA. [8]
- b) Discuss the design of a typical input or output interface. [8]
7. a) Describe in detail about pipeline processing. [8]
- b) Write short notes on Interprocessor Communication and Synchronization. [8]