Code No: **R41021**   **R10**   **Set No. 1**

IV B.Tech I Semester Supplementary Examinations, February - 2019
COMPUTER ORGANIZATION
(Electrical and Electronics Engineering)

Time: 3 hours   Max. Marks: 75

Answer any FIVE Questions
All Questions carry equal marks
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1 a) What are the basic Functional Units of a Computer System?   [8]
   b) Explain about Bus Structure and how the bus is connected between processor and main memory?   [7]

2 a) Discuss about Common Bus System of basic computer Registers and memory.   [8]
   b) What is instruction cycle? Explain the Flow chart for instruction cycle.   [7]

3   Explain about different Addressing Modes with examples.   [15]

4 a) What is a micro program sequencer?   [6]
   b) Differentiate between Hardwired control and Micro programmed control.   [9]

5   Discuss in detail about Cache memory mapping techniques with neat diagram.   [15]

6   Explain the operation of DMA with neat diagram and also discuss about the DMA operating modes.   [15]

7 a) Explain about RISC pipeline.   [5]
   b) What is Pipelining? Explain pipeline processing with an example.   [10]

8   Explain the following
        a)   Serial Arbitration Procedure
        b)   Parallel Arbitration Logic
        c)   Dynamic Arbitration Algorithms.   [15]