Code No: H5503/R13

M. Tech. II Semester Regular/ Supplementary Examinations, July-2016

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

(Embedded Systems)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain the various architectures of Xilinx Cool Runner CPLDs.	8
	b	Distinguish between programmable logic devices.	4
2.	a	Write short notes on CPLD implementation of a parallel adder with accumulation.	7
	b	Realize 3X8 decoder with single enable input using PAL & PLA.	5
3.	a	With neat diagrams, explain logic block architectures of FPGAs.	8
	b	Write short note on applications of FPGAS.	4
4.	a	Write about SRAM Programming technology of programmable FPGAs with neat sketches.	7
	b	List out the salient features of Xilinx 3000 CLB.	5
5.	a	Discuss the architectural differences of Act1, Act2 family FPGAs.	7
	b	Explain about how anti-fuse programming technology used in Actel FPGAs.	5
6.	a	How would you implement a binary counter using the CLBs of FPGA?	8
	b	Describe applications of Actel FPGAs.	4
7.	a	Design Mod-6 counter using FPGAS and draw necessary diagrams.	8
	b	What are the general design issues of FPGAs in design applications?	4
8.	a	Explain about position tracker of a Robot manipulator with help of FPGAs.	8
	b	Realize full adder using Actel FPGAs.	4

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