Code No: H6804/R13

M. Tech. II Semester Regular/ Supplementary Examinations, July-2016

DESIGN FOR TESTABILITY

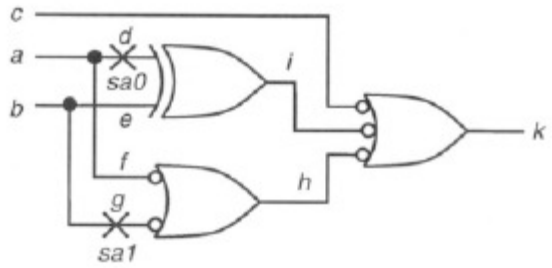
(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI&ME)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

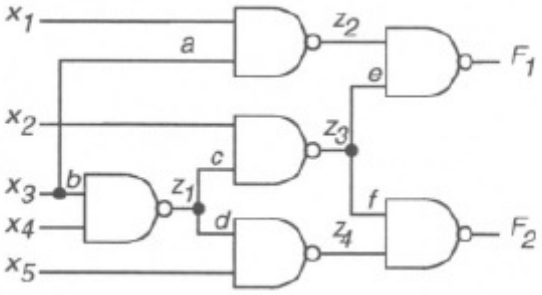
1. a What are the types of tests a VLSI chips are subjected to? Discuss. 6
   b Elaborate on typical defects in VLSI chips with examples. 6

2. a Show that the two faults d: s-a-0 and g: s-a-1 are equivalent in the figure below: 6



   b Explain, with a block diagram, simulation for design verification. 6

3. a Explain why the reverse order fault simulation is not a practical test compaction technique for sequential circuits. 6
   b For the circuit shown in figure, compute the combinational SCOAP testability measures, both controllability and observability. 6



4. a How a mutual comparator useful for memory BIST? Explain. 6
   b With a block diagram, explain full circular BIST configuration. 6

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5.	a	What is the advantage of weighted pseudo random pattern generator over the normal method?	6
	b	What is the advantage of pseudo exhaustive pattern generator over exhaustive pattern generator?	6
6.	a	Explain the test procedure for syndrome-testable circuit with suitable block diagram.	6
	b	What is STUMPS? Explain how this BIST architecture is special?	6
7.	a	Explain the advantages of boundary scan description language.	6
	b	With state diagram and timing waveforms, explain the TAP controller design.	6
8.	a	Discuss functional Vs structural testing.	6
	b	Write a note on ad hoc DFT methods.	6

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