Code No: H6806/R13

M. Tech. II Semester Regular/ Supplementary Examinations, July-2016

SYSTEM ON CHIP DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID , VLSI, VLSID, VLSISD, VLSI & ME, ES and DS & CE)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain the flow of SoC design Approach.	6
	b	Compare SoC multiprocessors and multi threaded processor.	6
2.		Find a SoC configuration that uses a Vector processor and describe the architecture of the vector processor.	12
3.		What are the basic cache organizations? Explain in detail.	12
4.	a	List all the operations that must be performed after a "not-in-TLB" signal.	6
	b	How would a designer minimize the "not-in-TLB" penalty?	6
5.	a	List the standard SoC buses. Explain AMBA?	8
	b	Compare AMBA and Core Connect Busses.	4
6.	a	What are the motives of reconfiguration? Explain trade off analysis.	6
	b	Explain CUSTARD micro architecture.	6
7.	a	Explain Stretch S6 software configurable processor engine.	6
	b	List the different types of reconfigurable interconnects. Explain each briefly.	6
8.		Explain in detail the JPEG system for digital still camera.	12

*****