Code No: G6806/R13

M. Tech. I Semester Supplementary Examinations, January-2017

DIGITAL SYSTEM DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME, ES, DE&CS, E&CE and DECE)

Time: 3 hours **Max. Marks: 60**

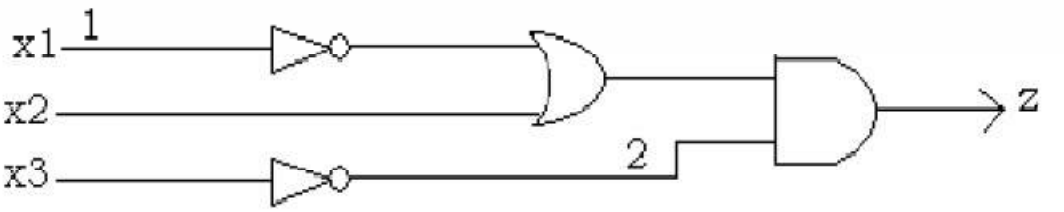
Answer any FIVE Questions
All Questions Carry Equal Marks

1. a List out the cube based operations that can be used in cube based minimization algorithm and explain them with an example each. 6M
   b Apply CAMP algorithm to minimize the given 4 variable Boolean function 6M
   f (a, b, c, d) = ∑m (1, 3, 5, 7, 9, 10, 13, 14, 15)

2. a Implement the following Boolean functions using PLA 6M
   F1 (X, Y, Z) = ∑ (1, 2, 4, 6) F2 (X, Y, Z) = ∑ (0, 1, 6, 7) F3 (X, Y, Z) = ∑ (2, 6)
   b List out the steps to be consider for PLA folding algorithm? 6M

3. a Design a combinational circuit using a ROM. The circuit accepts a 3 bit number and generates an output binary number equal to the square of the input number. 8M
   b How a sequential circuit can be designed using FPGA? 4M

4. a Using the path-sensitization method and Boolean difference method find the test vectors for SA0 fault on input line 1 and SA1 fault on the internal line 2 of the circuit shown in figure 8M



   b Write a short note on Fault classes and Models? 4M

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5. a

Ps	Ns, z x=0 , x=1	
A	B,0	D,0
B	A,0	B,0
C	D,1	A,0
D	D,1	C,0

Conduct a Homing experiment and determine shortest homing sequence which identifies the final state of the given state machine. 8M

b Explain the properties of a successor tree. 4M

6. a Simplify the Boolean expression using k-map 6M
F = πM (0, 1, 3, 5, 6, 7, 10, 14, 15)

b Compare PROM, PLA and PAL. 6M

7. a Discuss the BIST scheme for PLD and CPLDs. 6M

b Classify the fault detection experiments for the sequential circuits with examples. 6M

8. Draw an ASM chart to design control logic of a binary multiplier. Realize the same using MUX, decoder and D-type flip flops. 12M

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