Code No: I6804/R16

M. Tech. I Semester Regular Examinations, January-2017

HARDWARE SOFTWARE CO-DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a Explain the FSM model for elevator controller.
   b Explain CISC architecture with neat sketch.

2. a Discuss the parallel architecture.
   b List and explain the different concurrencies.

3. a Explain the prototyping and emulation techniques.
   b Describe the Aptix prototyping system.

4. a Discuss the 8051 an 8-bit microcontroller architecture.
   b Explain mixed systems and less specialized systems.

5. a Discuss the optimizations for embedded processor.
   b What is compiler validation? Explain.

6. a Explain blocking versus non blocking operations.
   b Write about Interface verification.

7. a Discuss the system level specification languages.
   b Explain the architecture oriented intermediate forms.

8. a Explain the automatic generation of cosimulation interfaces.
   b Discuss the COSYMA design flow and user interaction.

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