Code No: H6805/R13

M. Tech. II Semester Supplementary Examinations, May-2017

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURE

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME, SSP, DIP, CE&SP, IP, C&SP, SP&C, ES, DS&CE, DECS, E&CE, DECE and CS)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

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1. a Draw and explain the block diagram of a Digital Signal-Processing system. [6M]
   b What are the different number formats that are used to represent signals and coefficients in DSP systems? Explain any two of them. [6M]

2. Discuss in brief about the data addressing capabilities of programmable DSP devices with examples. [12M]

3. Describe the following on-chip peripherals of TMS320C54xx processors. 6M X 2 = 12M
   (a) Hardware Timer
   (b) Host port interface

4. a Write a brief note on Micro Signal architecture. [4M]
   b Explain in detail about Blackfin processor. [8M]

5. a Draw and explain the block diagram of memory interface for TMS320C5416 processor. [6M]
   b How does DMA help in increasing the processing speed of a DSP processor? [6M]

6. a Explain in brief about errors in A/D conversion process. [6M]
   b Explain the concept of Pipelining for speeding up the execution of an instruction. [6M]

7. a Describe the operation of the following instructions: [6M]
      (i) MAS *AR3- , *AR4+, B, A
      (ii) MAC *AR1+ , *AR2- , A
   b Discuss in brief about the basic peripherals in analog devices family of DSP devices. [6M]

8. Write short notes on any **TWO** of the following: 6M X 2 = 12M
   (a) Parallel I/O Interface
   (b) Memory map of TMS320C5416
   (c) Barrel Shifter

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