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Code No: H6810/R13

M. Tech. II Semester Supplementary Examinations, May-2017

SEMICONDUCTOR MEMORY DESIGN & TESTING

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI&ME)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Discuss the soft errors failures in DRAM.	6M
	b	Compare 4MB and 16MB SRAM, advanced SRAM architectures and their designs	6M
2.	a	Explain the architecture of a 256K CMOS flash memory.	6M
	b	Explain about high density (multi MB) ROMs	6M
3.	a	Explain the following (i) stuck –at fault (ii) Bridging fault (iii) Coupling faults	6M
	b	Write about pseudo Random testing of a RAM.	6M
4.	a	Explain various radiation hardening design issues.	6M
	b	Explain about single event phenomenon with respect to radiation effects.	6M
5.	a	Explain the FRAM cell and its memory operation.	6M
	b	Write short notes on (i) flash memory cards (ii) CMOS SRAM card.	6M
6.	a	Discuss about TRENCH and stacked capacitor cells inn DRAM.	6M
	b	Discuss about non volatile memory radiation characteristics.	6M
7.	a	Explain about wafer radiation testing and test structures.	6M
	b	Write a short notes on 3D memory stacks and MCMs.	6M
8.	a	Explain about floating gate EPROM cell with a neat sketch.	6M
	b	Briefly explain about BIST techniques for memory.	6M

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