

Code No: J6802/R16

M. Tech. II Semester Regular Examinations, May-2017

CMOS MIXED SIGNAL CIRCUIT DESIGN

**Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81)
 VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76),
 Embedded Systems (55)**

Time: 3 Hours

Max. Marks: 60

*Answer any FIVE Questions
 All Questions Carry Equal Marks*

1. a What is switched capacitor? What is its significance in the CMOS technology? 5
 b If $C_1 = C_2 = C$, find the value of C that will emulate a $1M\Omega$ resistor if the clock frequency is 200 KHz. 7
2. a Explain about the basic charge pump PLL with a neat figure. 5
 b With the help of necessary waveforms, explain about the non-ideal effects in PLLs. 7
3. a What are the dynamic characteristics that influence the performance of DACs? 5
 b Design a decoder based DAC with a detailed explanation. 7
4. a Give the classification of ADC architectures based on the conversion rate. 5
 b Explain the static and dynamic characteristics of ADCs. 7
5. a What is a flash converter? Explain the function of a 3 bit flash ADC. 5
 b What is time interleaving? Explain the operation of a time interleaved ADC. 7
6. a Discuss about Delta-Sigma ADC. 5
 b Explain the block diagram of second order Delta-Sigma modulator. 7
7. Distinguish between oversampling without noise shaping and with noise shaping. 12
8. a What are biquad filters? Explain about the two switched capacitor biquad realizations. 5
 b Design a switched capacitor realization for a first order, high pass circuit with a high frequency gain of -10 and a -3dB frequency of 1 kHz using a clock of 100kHz 7
