Code No: J6805/R16

M. Tech. II Semester Regular Examinations, May-2017

DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76), SSP (45), DIP (63), CE&SP (46), IP (-), C & SP (80), Embedded Systems (55), Digital Systems & Computer Electronics (06), DECS (38), ECE (70), DECE (37), Communication Systems (47), Instrumentation And Control Systems (27)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Draw and explain the block diagram of a Digital Signal-Processing system.	[6M]
	b	What are the different number formats that are used to represent signals and coefficients in DSP systems? Explain any two of them.	[6M]
2.		Discuss in brief about the data addressing capabilities of programmable DSP devices with examples.	[12M]
3.		Describe the following on-chip peripherals of TMS320C54xx processors. (a) Hardware Timer (b) Host port interface	6M X 2 = 12M
4.	a	Write a brief note on Micro Signal architecture.	[4M]
	b	Explain in detail about Blackfin processor.	[8M]
5.	a	Draw and explain the block diagram of memory interface for TMS320C5416 processor.	[6M]
	b	How does DMA help in increasing the processing speed of a DSP processor?	[6M]
6.	a	Explain in brief about errors in A/D conversion process.	[6M]
	b	Explain the concept of Pipelining for speeding up the execution of an instruction.	[6M]
7.	a	Describe the operation of the following instructions: (i) MAS *AR3- , *AR4+, B, A (ii) MAC *AR1+ , *AR2- , A	[6M]
	b	Discuss in brief about the basic peripherals in analog devices family of DSP devices.	[6M]
8.		Write short notes on any **TWO** of the following: (a) Parallel I/O Interface (b) Memory map of TMS320C5416 (c) Barrel Shifter	6M X 2 = 12M

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