Code No: J6809/R16

M. Tech. II Semester Regular Examinations, May-2017

CPLD AND FPGA ARCHITECURES AND APPLICATIONS

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81) Embedded Systems (55)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a With neat sketch explain Altera max 5000 series CPLD
   b What is a structured ASIC? How does this compare and differ from the traditional ASIC and the PLD?

2. a Explain problems associated with designing with FPGAs and also discuss some common issues?
   b What is an FPGA? Give the advantages and disadvantages of FPGA?

3. a Draw and explain Simple SRAM-Programmable FPGA Architecture
   b Draw and explain the Xilinx XC2000 Architecture?

4. a Describe in detail how segmented routing is applied in the ACT FPGA routing architecture?
   b With an example explain State Machine Design using Act1 modules?

5. a Design a 6-bit synchronous loadable binary counter with a count enable using Act2 FPGA?
   b How would you implement the function Y = A + B + C using Actel Act1 FPGA?

6. a What are the salient features of XC4000 FPGA CLB?
   b Write short notes on CPLD implementation of a parallel adder with accumulation

7. a Explain about position tracker of a Robot manipulator with help of FPGAs
   b How would you implement a Melay machine using a CPLD?

8. Write short notes on:
   a. Design flow for FPGA implementation.
   b. Meta stability

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