Code No: G6802/R13

M. Tech. I Semester Supplementary Examinations, JAN/FEB-2018

VLSI TECHNOLOGY AND DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME, DS&CE, DE&CS, E&CE and DECE)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	What is Moore's law? Explain its relevance with respect to evolution of technology?	6M
	b	What are design rules? Explain the different types of design rules and give some examples?	6M
2.	a	What are the various masks used in CMOS p-well process? What is the significance of each?	6M
	b	What are the differences between CMOS and BiCMOS technologies in fabrication?	6M
3.	a	Derive an equation for transconductance of an n-channel enhancement MOSFET operating in active region?	6M
	b	What is sheet resistance? Derive the Expression for R_S? Calculate the ON resistance from V_{DD} to GND for the nMOS and CMOS inverter circuits.	6M
4.	a	Derive the relation between I_{DS} and V_{DS} of MOSFET.	6M
	b	Write the scaling factors for different types of device parameters.	6M
5.	a	Draw the basic structure of a dynamic CMOS logic and explain the same?	6M
	b	Compare Two-phase clocking system with single phase clocking system? Explain the operation of clocked inverter circuit with suitable diagram?	6M
6.	a	What are the need for testing and explain the two categories for testing.	6M
	b	What is SOCs? Give some examples of it?	6M
7.	a	What is mean by floor planning? Explain the different methods of floor planning.	6M
	b	Design a circuit for input pad connectivity and explain its necessity in chip design.	6M
8.	a	Write short notes on i) Resistive and inductive interconnect delay ii) High level Synthesis	12M

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