Code No: G6803/R13

M. Tech. I Semester Supplementary Examinations, Jan/Feb-2018

CMOS ANALOG IC DESIGN
(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD, VLSI&ME)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Explain about the CMOS device Modeling	6M
	b	Explain about the computer simulation models	6M
2.		What is Current Mirror .Explain the general properties of current mirrors with block diagram	12M
3.	a	Explain the difference between cascade current mirror and Wilson current mirror	6M
	b	Write a short notes on current sinks and sources	6M
4.	a	Explain about the design of CMOS opamps	6M
	b	Derive the expression for power-supply rejection ratio of Two-stage op-amps	6M
5.	a	Differentiate the Two-stage comparator and Discrete time Comparator	6M
	b	Explain about the different types of Open loop comparator	6M
6.	a	Explain about the design of Two-stage op-amps	6M
	b	Explain about the Cascode Op-amps	6M
7.	a	Explain about the Delay Locked Loops	6M
	b	Discuss about the Oscillator applications	6M
8.	a	Define Oscillator. Explain about the Ring Oscillator with an example	6M
	b	Discuss various types of open loop comparators	6M

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