

Code No: G6804/R13

M. Tech. I Semester Supplementary Examinations, JAN/FEB 2018

**CPLD AND FPGA ARCHITECTURES AND APPLICATIONS****Common to VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76), VLSI&ES(68), ES&VLSI(48), VLSID&ES(77), ES&VLSID(81)****Time: 3 Hours****Max. Marks: 60**

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*Answer any FIVE Questions*  
*All Questions Carry Equal Marks*

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1. a Implement a BCD to Excess-3 code converter by ROM. Calculate the cross point density of the implementation? 6M  
b Explain few differences between programmable logic device and Complex programmable logic devices? 6M
2. a Explain the concept of Programmable I/O blocks in FPGAs? 6M  
b Briefly discuss about the applications of FPGA? 6M
3. a What is a Trade-off? Discuss about the different design Trade-offs? 6M  
b Draw and explain the CLB and IO Blocks of Xilinx XC2000 architecture? 6M
4. a How the ACT3 architecture is different from ACT2 architecture? Explain the ACT3 architecture in detail. 6M  
b Explain the ACT2 architecture for high fan-in example? 6M
5. a Design a five bit binary counter with ACT devices? 6M  
b Write a short note on a position tracker for a robot manipulator? 6M
6. a With neat block diagram, explain the architecture of Xilinx Cool Runner XCR3064XL CPLD? 6M  
b When is CPLD better suited than SPLD? List out the comparisons between those two. 6M
7. a Tabulate the comparisons of different XC3000 family members? 6M  
b Write a short note on Programming Technology? 6M
8. a Write a short note on 12M  
i) Duplicated logic ii) Clock enables iii) Iterative design methodologies

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