Code No: G6809/R13

M. Tech. I Semester Supplementary Examinations, Jan/Feb-2018

CMOS DIGITAL IC DESIGN

(Common to VLSI & ES, ES & VLSI, VLSID & ES, ES & VLSID, VLSI, VLSID, VLSISD and VLSI&ME)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. a Define Threshold Voltage. Express threshold voltage and discuss dependency of VT on various parameters.
   b Explain the DC noise margin of CMOS logic.

2. Design and implement CMOS full adder circuit.

3. Design and implement AOI and OIA using CMOS.

4. Realize NMOS complex logic gates using the Boolean function Z=A(D+C)+BE.

5. a Discuss the transient analysis of CMOS Transmission gate by replacing it with resistor equivalent circuit. Design an EX-OR gate using Transmission gate Logic.
   b Design an EX-OR gate using Transmission gate Logic.

6. a Draw the D latch by using CMOS logic and explain its operation in detail.
   b Write short notes SR latch in sequential MOS logic.

7. Mention different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM cell.

8. a Compare the performance of SRAM and DRAM.
   b Write about dynamic pass transistor.

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