Code No : I6801/R16

M. Tech. I Semester Regular/Supple Examinations, Jan/Feb-2018

DIGITAL SYSTEM DESIGN
(Common to VLSI&ES, ES&VLSI, VLSID&ES, ES&VLSID, VLSI, VLSID, VLSISD, VLSI&ME, ES, DE&CE, DE&CS, E&CE, C&CE, C&C and I&CS)

Time: 3 hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1. Minimize the following switching function using CAMP Algorithm.
   f (a, b, c, d) =$\sum$ m (1, 3, 5, 7, 9, 10, 13, 14, 15) 12M

2. Determine the Essential Prime Cubes for the following four variable single output function using IISc Algorithm.
   f = 0200 + 1102 + 2201 + 0011 + 0010 12M

3. Find a simple column PLA folding of the following SSR Table and draw the folded PLA. 12M

Columns	SSR
A	14
B	1, 3
C	3, 4, 5, 9, 12
D	1, 2, 5, 10, 11, 15
E	2, 4, 7, 8, 10, 15, 16
F	1, 2, 15
G	6, 8, 11, 13
H	3, 5, 6, 14, 15
I	7, 10, 12, 13, 16
J	4, 9, 16

4. Determine the minimal test set to detect various faults for a given PLA which is having four inputs (x_1, x_2, x_3 and x_4), two outputs (z_1 and z_2) and five product terms (p_1, p_2, p_3, p_4 and p_5) The functions realized are 12M

   $Z_1 = p_1 + p_2 + p_3$
   $Z_1 = x_1^1 x_3^1 + x_3^1 x_4 + x_1 x_3$
   $Z_2 = p_2 + p_4 + p_5$
   $Z_2 = x_3^1 x_4 + x_2 x_3 x_4^1 + x_1 x_2 x_3$

5. Determine the distinguishing sequence for the following machine M by conducting adaptive distinguishing experiment. 12M

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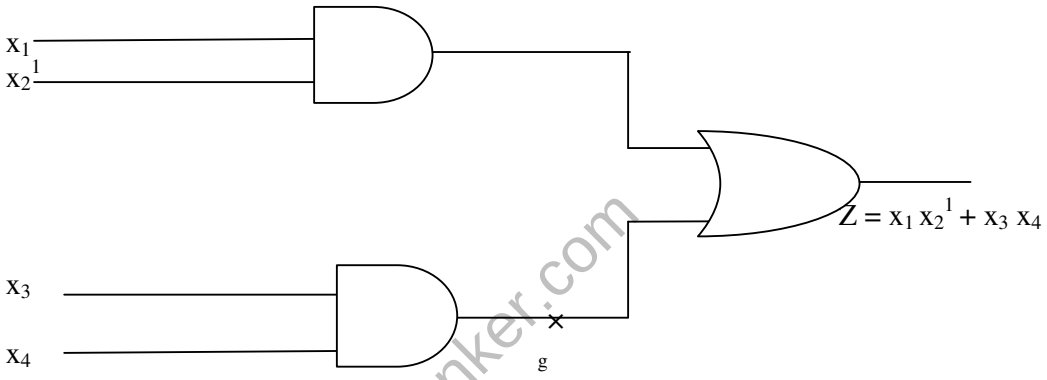
Machine M

PS	NS, Z	
	X = 0	X = 1
A	D, 0	C, 0
B	C, 1	D, 1
C	B, 1	A, 0
D	A, 0	A, 0

6. A Two Level AND – OR logic circuit has two AND gates feeding one OR gate. The two AND gates realize the product terms $x_1 x_2^1$, $x_2 x_3$ respectively. Derive the a and b tests for detecting SA1 fault on the line x_2^1. Find a minimum test set for the network shown.

12M



7. Design a digital system with two Flip-flops E and F and one 4 bit binary counter A. The individual flip flops in A are denoted by A_4, A_3, A_2 and A_1 with A_4 holding the most significant bit of the count. A start signal S initiates the system operation by clearing the counter A and flip flop F. The counter is then incremented by one starting from the next clock pulse and continues to increment until operations stop. Counter bits A_3 and A_4 determine the sequence of operations: if A_3=0, E is cleared to Zero and the Count Continues. If A_3=1, E is set to 1; then if A_4=0, the count continues, but if A_4=1, F is set to one on the next clock pulse and the system stops counting.

12M

8. Write notes on any Two of the following. 12M
   (a) ROM Design
   (b) Kohavi Algorithm
   (c) DFT schemes

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