Code No: I6802/R16

M. Tech. I Semester Regular/Supple Examinations, Jan/Feb-2018

VLSI TECHNOLOGY AND DESIGN

Common to VLSI&ES (68), ES&VLSI (48), VLSID &ES (77), ES &VLSID (81), VLSI (57), VLSID (72), VLSI System Design (61), VLSI & Micro Electronics (76),DSCE(06), DECS(38), ECE (70), DECE (37), and Instrumentation And Control Systems (27)

Time: 3 Hours **Max. Marks: 60**

Answer any FIVE Questions
All Questions Carry Equal Marks

1.	a	Draw and explain VLSI design process in detail.	6M
	b	Write a short notes on (i) CVSL(ii)pseudo n MOS	6M
2.	a	Design CMOS using twin tub process	8M
	b	Discuss the need of a BICMOS technology.	4M
3.	a	Derive the voltage and current relationship of a MOS in different regions.	6M
	b	Write the effects of scaling on at least 10 parameters.	6M
4.	a	Discuss the clock skew with example.	6M
	b	Design 4X4 barrel shifter.	6M
5.		Discuss (i) global routing (ii)power distribution (iii) clock distribution.	12M
6.		Draw and explain (i) I/O architecture (ii)pad design .	12M
7.	a	Discuss the need of a mixed signal design in VLSI.	6M
	b	Compare the performance of different fabrication processes.	6M
8.		Discuss in detail the low power architectures.	12M

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