Code No: MC1312/R13

MCA I Semester Supplementary Examinations, January-2018

DIGITAL LOGIC AND COMPUTER ORGANIZATION

Time: 3 Hours **Max. Marks: 60**

Answer Any **FIVE** *Questions*
All Questions Carry Equal Marks

1.	a	Convert the following binary number to their equivalent decimal and hexadecimal (base 16) representation. i) 101101.0101 ii) 1010.0111 iii) 10.01	6M
	b	Discuss the Logic Gates with neat sketches.	6M
2.	a	Explain DTL and TTL NAND Gates.	6M
	b	Realize the expression g = a.b.c' + d + f ' + a.e' using NAND gates.	6M
3.	a	Perform the following arithmetic operations assuming that the decimal digits are coded in 8421 code i)24+16 ii) 12+13 iii) 84 - 97	6M
	b	Explain a Four-bit Adder with neat sketch.	6M
4.	a	Define addressing mode? Explain direct addressing mode with example.	6M
	b	Write the features of SMAC2.	6M
5.	a	Define ROM? Explain it.	6M
	b	What is Interrupt? Explain Single level Interrupt Processing.	6M
6.		Draw the functional block diagram of Dynamic Random Access Memory and explain it.	12M
7.	a	Define Control Memory? Explain Micro program Sequencer.	6M
	b	Write a note on register sets.	6M
8.		Design the combinatorial circuits with multiplexers.	12M

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